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Fast Prototyping of Analog ICs Using Transistor Arrays

Michel J. Declercq

Wheras in the digital world CAD tools and the various techniques of prediffused transistor arrays have been successfully applied to VLSI-development, with very few compromises on performance, the analog world could not keep in step. Main reasons for that are the infinite variety of specifications and the constraints that are typical for analog circuits. The development time and cost was more important than the processing costs, reducing so the advantage of using transistor arrays. The recent appearance of a new generation of smart analog tools is actually changing this situation, giving a new interest to array-based design. After reviewing the design basis of the actual analog arrays, their architecture philosophy and trade-offs will be discussed for various technologies. Circuit design techniques and analog CAD tools dedicated to prediffused arrays will finally be presented.

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Since the early times of integrated circuits, full-custom design has been used as the optimal solution in terms of speed and small area. In the era of integrated VLSI systems, and with an evolving trend for ASICs, this design style is however almost unaffordable due to time and cost of both design and processing. Solutions to this problem have been found by new developments in the direction of design methodologies, CAD tools, and prediffused transistor arrays. These techniques have been successfully applied to digital VLSI, for which true silicon compilation is almost a reality. Moreover, advanced sea-of-gates techniques provide a fast and cheap access to silicon, with very few compromises on performance, except for the silicon area.

In the analog world, things did not move that fast for several reasons. Cell libraries have a limited use, owing to the infinite variety of specifications and constraints that are typical for analog circuits. Cells generators have been proposed, but these are usually restricted to a few circuit families and to a few technologies. The concepts of structured and hierarchical design, that have proven to be so successful in digital design, are not so widely applicable for complex analog circuits, especially when global parameters such as noise, offset, dynamic and linearity are critical issues. Analog design having long been an art as well as a science, the development time and cost were important compared to digital systems. In this framework, the impact of processing costs was relatively lower, reducing the advantage of using transistor arrays in analog design. Moreover, most analog designers being very conservative, they where quite reluctant to use a design style that reduced their degree of freedom due to the quantified character of a prediffused array.

A major effort is actually under way in several research and development groups to create a new generation of smart analog tools. As fast and cheap prototyping is becoming more and more critical in ASICs development, mentalities are now evolving, and new generations of analog arrays in various technologies are receiving more and more acceptance in the analog world. As a matter of fact, analog arrays can provide key advantages that overcome many of their limitations. Advanced technologies such as Bicmos or full-dielectric isolation (D.I.) Bipolar would never be affordable for custom applications in another form than prediffused arrays. Personalization steps usually require 4 to 5 masks, combined with non-critical operations such as the interconnection metal layers. On the other hand, a full process may require as many as 16 or 18 masks, the most critical and expensive operations being located at the front end of this process.

Design Basis of Analog Arrays

Basic Features of MOS and Bipolar Devices as Analog Circuits Components

Bipolar technology has been for long the favorite choice for analog integrated circuits. Its most important characteristics are summarized in the analytical expression of the collector current I_c and of the transconductance gm:

$$I_C = I_S \cdot e^{\frac{V_{BE}}{kT}} \qquad (1a)$$

Bipolar transistors enjoy a good matching when realized on the same silicon substrate, because this match-

ing depends mainly on physical parameters rather than geometrical parameters. The emitter area appears as a coefficient in the saturation current I_s, while the base-emitter control voltage V_{BE} is located in the exponential term. The transconductance is very high, and varies linearly with I_c. The output conductance g_{ce} is low, the early voltage being in the range of 40 to 100 V for common technologies. Finally, the current driving capability of bipolar transistors is usually larger (by a factor of about 5) than for MOS devices of identical area. On the other hand, bipolar transistors suffer from some limitations too. Among them, the non-infinite input impedance, the need for a base polarization current, and the wasted area due to collector isolation are the most frustrating in analog design. The fundamental expressions of the drain current of MOS transistors are

$$g_m = I_C \cdot \frac{q}{kT} \tag{1b}$$

for the linear region:

$$I_D = \beta \cdot \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2a}$$

for the saturation:

$$I_D = \frac{\beta}{2} (V_{GS} - V_T)^2 \tag{2b}$$

while the transconductance is given by

$$g_m = \beta \cdot (V_{GS} - V_T) = \sqrt{2 \cdot \beta \cdot I_D} \tag{2c}$$

with

$$\beta = \mu \cdot C_{OX} \cdot \frac{W}{L} \tag{2d}$$

It readily appears that MOS performance is much more sensitive to technology, and directly depends on the geometrical size of the devices. The transconductance of an MOS transistor is more than one order of magnitude lower than its bipolar counterpart at identical size. The output conductance of MOS transistors is also usually rather poor, and directly depends on the channel length L. Moreover, the 1/f noise may be critical for low-frequency amplifiers.

Initially, MOS technology was therefore considered for analog circuits only when small analog blocks had to be combined with CMOS logic on the same substrate. With MOS analog circuit techniques reaching maturity, many new advantages have been found that largely balance the drawbacks. As a matter of fact, MOS devices can be used as resistors as well as control devices, they present a high input impedance, have an inherent dynamic memory capacity, and can be used as efficient switches for both voltage and current. Switched capacitor techniques have proven their high efficiency for filtering as well as for A/D or D/A conversion.

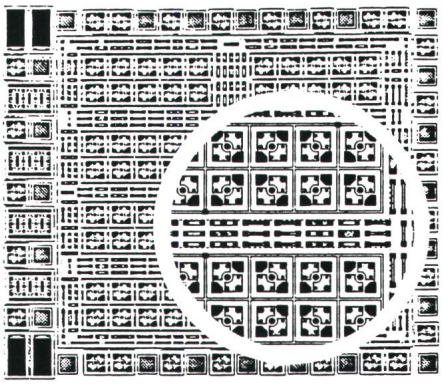

Figure 1 Bipolar analog transistor array (Ascom Microelectronics)

MOS analog circuits are now considered as interesting alternatives to bipolar in many applications. For this reason attention is now given to MOS analog transistor arrays, as described later. This short analysis also shows that the combination of both worlds in a state-of-the-art Bicmos technology opens a new era in analog design, including array-based designs.

Device-level Requirements for Analog IC Technologies

Besides the general requirements of any analog IC technology, such as compatibility with high-density logic, device matching, low-noise, medium- to high-voltage capability, etc., some desirable features can be specified for each technology on the basis of the considerations discussed hereabove. In MOS, those are for instance the free choice of device size (W and L), the availability of high-quality capacitors, the floating-well capability, the availability of some CMOS-compatible lateral bipolar devices. In bipolar, good pnp-transistors, high-quality resistors, J-FETs and low-resistance cross-overs should be available.

Analog Arrays Architectures

Bipolar Arrays

Trends in analog bipolar arrays directly reflect the conclusions hereabove. The core of the array contains fixed-size transistors and a variety of resistor values, while some special components such as power transistors, capacitors, etc., are located at the periphery. In order to provide for a structured, modular design approach, transistors are usually grouped in blocs of 10 to 20, called tiles, surrounded by resistors. The ideal size of a tile should fit approximately the size of an analog subcircuit (voltage ref., comparator, buffer, amplifier, mixer, etc.).

In basic bipolar technologies, a much higher degree of freedom is obtained when each transistor can be used as a vertical npn as well as a lateral pnp, instead of being dedicated to one of those functions only. A good example of this philosophy is found in the Ascom array [1], where each tile is composed of 10 of these versatile devices, called twinstors (fig.1).

Advanced technologies feature full-D.I. isolation together with a much wide variety of high-performance devices such as true vertical pnps, J-FETs, zener diodes, and high-precision resistors (implanted and thin-film NiCr) [2; 3; 4]. Exceptional performance at an affordable cost is achieved with this type of array. Voltage capabilities range between 20 and 40 volts, while npn's cut-off frequency F_t use to be higher than 5 GHz (fig.2). Accurate models are available for the devices, owing to the reduced parasitics offered by D.I., and layout errors are restricted to custom routing. The wide variety of devices reduces, however, the degree of regularity and symmetry of the array, making it less compatible with auto place and route CAD tools.

CMOS and Bicmos Arrays

The architecture of CMOS arrays drastically differs from that of bipolar arrays. In most arrays, transistors have a regular size through the entire core. Complete freedom should therefore be allowed for making any combi-

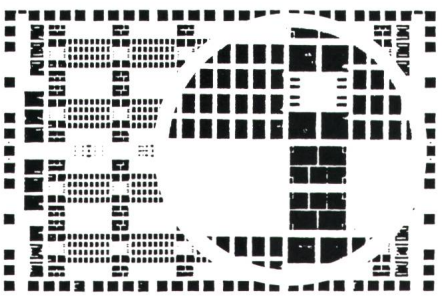

Figure 2 Complementary bipolar transistor array with full dielectric isolation Sipex

nation of serial and parallel connections of basic transistors, in order to simulate larger transistors with various W and L values. This feature gives the freedom to change the overall device transconductance, to increase its output conductance, to reduce the noise, and to select the appropriate trade-off between matching, silicon area and speed. Arrays are therefore made of

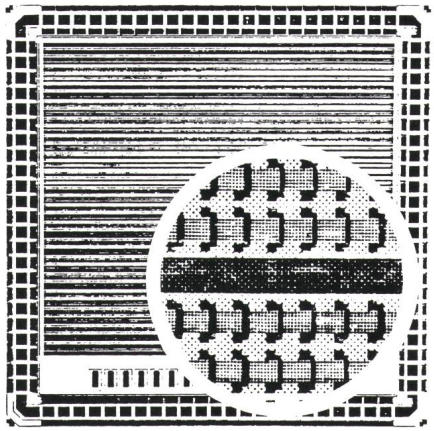

Figure 3 EPFL CMOS SOG array for analog and digital applications
a. Overall view of the array. The row of 16 large-size N-MOS transistors at the bottom are high-voltage (100 V) output devices.
b. Detail of the architecture. The basic cell is made of 2 N-MOS and 1 P-MOS transistors

continuous rows of transistors of both types, without any routing channel. Device isolation is based on the gate isolation method, commonly used in digital sea-of-gates arrays. In analog-compatible CMOS arrays, it is mandatory that the gates of n-channel and p-channel devices are not connected together, i.e. are not made out of a single poly-silicon stripe.

Figure 3 gives an example of an array designed at EPFL according to this philosophy, and usable for mixed analog-digital designs [5]. Symmetry, as well as full-transparency for routing through the cells in both directions, are key features for the analog performances of the array. Resistors are not available as such in the core of the array, except the low-ohmic poly-gate resistors. Designs must therefore be free of resistors, which is usually not critical except for some special circuits such as flash A/D converters or voltage references. Capacitors are more important for MOS design flexibility. Besides the junctions capacitances or the gate capacitances, which are fundamentally non-linear, a good solution has been found using contact pads areas as capacitors [6; 7]. The poly as well as the metal layers can be used to make a stack of capacitors that are mask programmable. These capacitors have been used successfully as compensation capacitors in amplifiers [8], or as charge storage devices in algorithmic A/D converters [9].

When a higher flexibility is needed, a special area of the array may be dedicated to special devices, such as a string of poly-resistors, a capacitor array, and some CMOS-compatible lateral bipolar transistors. A row of high-voltage NMOS or CMOS drivers, fully compatible with the standard low-voltage CMOS process, can also be located at the chip periphery (fig.3), [10]. Other array architectures that completely differ from the above principles have also been proposed. Most are dedicated to special applications such as SC filters. Combining the best of both worlds, Bicmos arrays open the way to high-performance semi-custom analog or mixed analog-digital designs. An example of such an array developped at EPFL within the frame of an Esprit-II project is shown in figure 4 [6].

Analog Circuit Design on Prediffused Arrays

Bipolar analog circuits built on transistor arrays exhibit characteristics that are very comparable to their full-custom version, except of course for the area. Trends are actually to propose a library of cells and subcells that fit in a tile, and are therefore preplaced and routed. This reduces the development time of the system, and gives an easy access to high-performance standard functions such as operational amplifiers or bandgap reference. A weak point of most bipolar analog arrays is the poor density achievable for the digital control blocks that are integrated on the same chip.

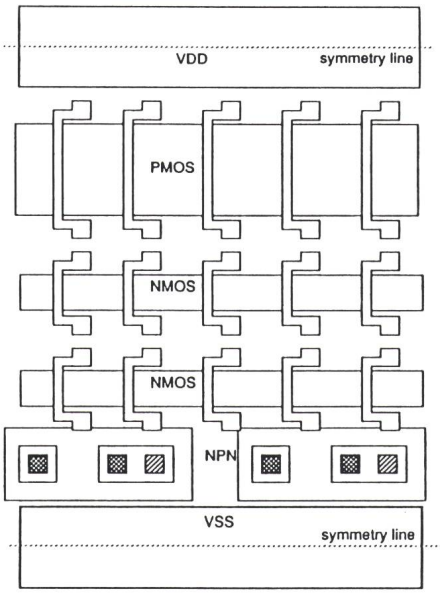

Figure 4 EPFL Bicmos SOG array (detail)

Differential pairs	type 1	type 2	type 3
average offset voltage (mV)	11.7	6.6	2.2
transconductance (μA/V)	130.4	140.1	141.8
output conductance (μA/V)	2.2	0.43	0.43
differential output conductance error	2.50%	2.41%	0.24%

Table I Characteristics of CMOS differential pairs realized on a CMOS transistor array
Type 1: Minimum-size transistors
Type 2: Combination of 5-parallel, 4-serial transistors, no-commmon centroid
Type 3: Combination of 5-parallel, 4-serial transistors, common centroid

MOS arrays, as stated before, can yield reasonable performance for analog circuits, using the appropriate technique. As a matter of fact, basic transistors use to be minimum-length devices and exhibit rather poor performance when used without precautions in critical parts of the circuits. The performance of basic building blocks implemented on a CMOS array can be significantly improved by using serial/parallel connections of basic devices, together with an appropriate symmetry of the layout configuration [7; 11]. Table I summarizes most important measurement results for differential pairs realized on a 2 μm-technology CMOS array. As expected, non-minimum differential pairs made of serial/parallel combinations have a much smaller offset voltage than pairs realized with single elementary transistors. The matching of output conductances, as well as their absolute values, are also much better.

The effect of serial connection of minimum-length devices on the overall output conductance is illustrated in table II for a 1.2 μm-technology. The output conductance effectively drops with the total channel length, but not as fast as for single long-channel devices as used in full-custom design. Table III summarizes the performances obtained for a classical operational

channel length (μm)	output conductance (μA/V)	
	single custom transistor	serial transistors
1.0	104	104
2.0	48	65
4.0	19	37
8.0	6	20

Table II Comparison between the output conductance obtained with a single long-channel custom transistor and a series of short-channel transistors

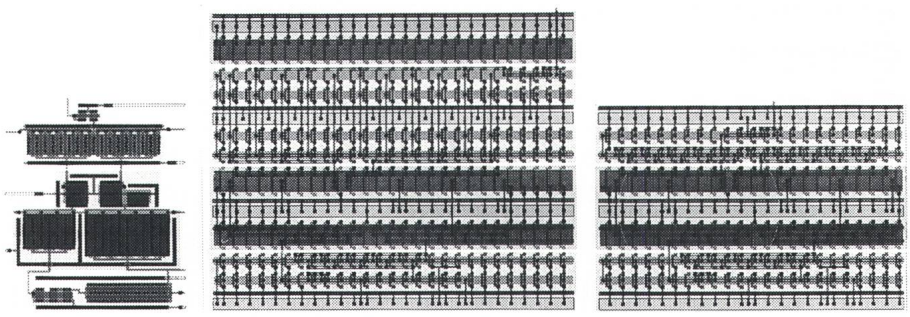

Figure 5 Layout comparison of 3 implementations of the same OTA
Left: Full-custom design; Center: Semi-custom design on EPFL CMOS SOG array (normal size); Right: Semi-custom design on EPFL CMOS SOG array (minimum size)

transconductance amplifier (OTA). For the sake of comparison, this circuit has been realized in 3 versions in the same technology: a full-custom layout, an array-based semi-custom version with the appropriate transistor sizes, and a second array-based version with minimum channel-length transistors (fig.5), [7]. Besides the increase in offset voltage and in silicon area, performances are very comparable between the full-custom and semi-custom versions, demonstrating that CMOS arrays are suitable for many non-critical mixed-mode applications.

Bicmos analog circuit performance is even less degraded compared to their full-custom version, due to the superior matching characteristics of bipolar transistors. Table IV summarizes the results obtained for a comparator and for an operational amplifier implemented on the EPFL Bicmos array.

Dedicated CAD Tools and Customization Steps

CAD tools have for long been the privilege of digital design, and if a few tools have appeared for analog full-custom, there has been almost nothing available for semi-custom analog design until very recently. For CMOS and Bicmos arrays, EPFL has developed a large set of tools including layout edition, cell generation, design verification and parameter extraction. Alps, an automatic place and route tool dedicated to the implementation of bipolar analog schematics on a transistor array, has been presented recently [12]. This tool actually supports a single custom metal layer, and takes into account several categories of user-imposed constraints. Harris Fastrack [4] is another example of a comprehensive set of software tools that enable the user to interactively design a bipolar analog IC, then estimate and optimize its yield.

For keeping their edge in fast prototyping, transistor or gate arrays must be processed using a fast and cheap method. Besides the classical photolithographic process, new fast and cost-effective solutions have appeared on the market. Direct-write E-beam and laser beam processing are now making a breakthrough in this area, and are making the array-based semi-custom approach still more attractive.

	unit	type 1	type 2	type 3
transconductance (mean value)	µA/V	96.5	108.1	92.0
transconductance (variance)	µA/V	3.9	4.0	9.3
linearity range	mV	103.1	100.0	122.1
offset voltage (mean abs. value)	mV	2.06	4.38	10.8
gain.bandwidth product	KHz	901	746	843
phase margin		68	53	60
slew-rate (C_L=5pF)	V/µs	1.05	1.3	1.3

Table III Compared results for 3 implementations of the same OTA
Type 1: Full custom
Type 2: CMOS array (normal size)
Type 3: CMOS array (min. size)

	Bicmos array	full-custom
Comparator		
max. frequency (MHz)	40	55
output fall time (ns)	8.5	3.5
OP-AMP		
gain.bandwidth (MHz)	18.4	15.1
phase margin	54	98
open-loop gain (dB)	86	86

Table IV Comparison of electrical results for Bicmos analog circuits

Conclusion

Analog semi-custom design on transistor arrays has emerged from a poor man's solution to a major design style, making fast prototyping possible at a reasonable cost, and even giving access to high-performance technologies that would not be affordable in any other design style.

Array regularity is the key for design flexibility, and is also the most appropriate for design automation. Array compatibility with mixed analog/digital designs is also an important feature, since most analog circuits need some type of control logic. Analog-compatible Bicmos arrays are basically combining the best features of MOS and bipolar. These high-performance arrays are particularly attractive for high-speed mixed analog/digital designs, such as used in telecommunication applications.

Array-dedicated CAD tools are only emerging, as far as analog applications are concerned; they may give a serious boost to analog semi-custom design. Whatever the technology of the array, the customization steps are simple and standard, and can therefore be processed locally. This interesting feature helps cutting both delay and price, while garanteeing a better design confidentiality. Moreover, overnight processing is now in sight with advanced customization processes such as laser-beam and E-beam lithography.

Switzerland enjoys a pole position in the analog semi-custom field. Several European Community contracts have been awarded in this field to both academic and industrial partners, confirming the interest for this attractive ASIC technology.

EPFL has been active since more than 4 years in the field of advanced Bicmos arrays for mixed analog/digital design, and is now pursuing a successfull industrial transfer of the results, while continuing research activities in dedicated design techniques and design automation tools.

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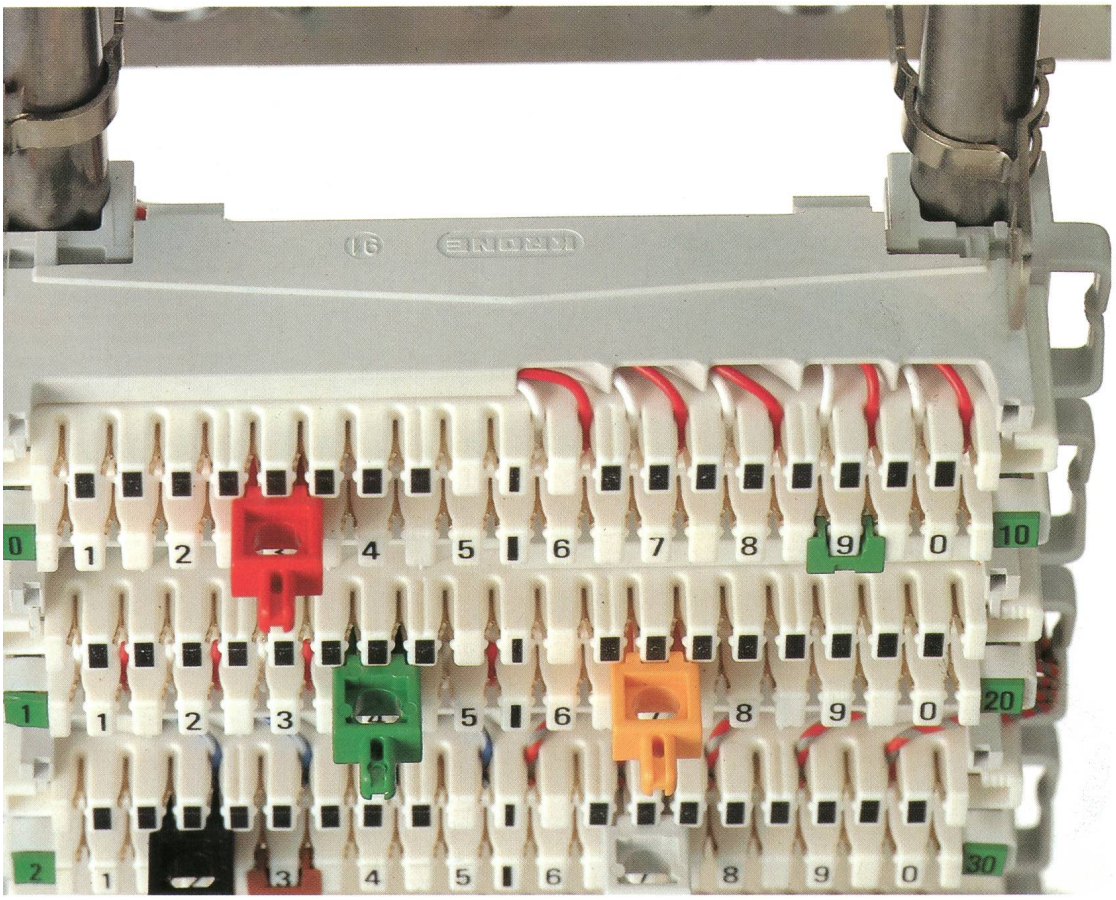

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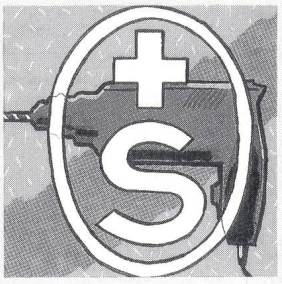

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