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Some Techniques of Pulse Code Modulation

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1. The Code

1.1 Introduction

The main advantage of pulse code modulation (PCM) is that the signals can be regenerated at frequent intervals. This usually involves amplitude slicing. Since in most cases it is not practical to transmit the dc level of the pulse train, the slicing level has to be found by means of two peak detectors, one for the positive and one for the negative peaks. These can only work, however, if one makes sure that both ones and zeros (pulse and no pulse) occur from time to time. This can be achieved, for example, by adding a special digit which is alternately zero and one. Even so, however, dc restoration remains a problem, especially at pulse rates of the order of 100 Mc/s and with noise superimposed on the signal.

This difficulty can be avoided by choosing a code in which the numbers of zeros and ones are balanced, so that there is no dc component to be restored. For this purpose one can start off with a "ternary" code, in which the digits represent powers of 3 instead of 2. Thus, each digit can assume either of the values 0, 1 or 2. (Alternatively, we may use +1, 0, −1.) Each ternary digit is then replaced by a pair of binary digits according to Table 1, and the result will be called the A-code.

Binary digits corresponding to the ternary code

Table I

Ternary	A-code	B-code
0	01	01
1	00	00 or 11
2	10	10

Here, the ternary 1 is represented by 00, but it could equally well have been 11 because this combination is still free. In the B-code, use is made of this fact by representing the ternary 1 by 00 or 11 alternately, that is once by 00, the next time by 11, and so on. It is easily seen that this code has the property that its mean value is always equal to 1/2 and that never more than 4 zeros or 4 ones follow each other.

With this "balanced" code, $N = 3^n$ amplitude levels can be represented, if $2n$ is equal to the number of digits. With 10 digits, $N = 3^5 = 243$, which is approximately the same as with an ordinary binary code of 8 digits, $N = 2^8 = 256$. Therefore, 2 additional digits are needed or 25% more bandwidth. (The asymptotic value of this ratio for large numbers of levels is (2 log 2) / (log 3) = 1.26.)

The advantages of a balanced code are the following:

1. Regenerative repeaters will be simpler because no dc restorers are needed. This is particularly important in a coaxial cable system because of the very large number of repeaters required. Also, it will be found that a repeater for a balanced code can work at a lower supply voltage level, thereby allowing more repeaters to be fed in series through the same cable.

2. All the amplifiers are uniformly loaded, and they need not be linear. Any amount of clipping is allowed so long as it is symmetrical. High-level microwave modulators can be driven from ac-coupled amplifiers. Coupling capacitors and transformers can be smaller.

3. The problem of the extraction of the pulse repetition frequency is simplified and timing errors due to level changes are reduced.

In some systems, such as FM radio links, there is not much advantage to be gained from a balanced code because the dc component can be transmitted without much difficulty. In this case the ternary code can be used directly, resulting in a bandwidth reduction. The following comparison shows approximately the relative bandwidth or number of digits required for various systems.

Balanced	*Binary*	*Ternary*	*Quaternary*
10	8	5	4

It will be found from this that by going from a binary to a ternary (3-level) code the bandwidth saving is considerable, whereas any further increase in the number of levels does not bring so much advantage, in view of the difficulties associated with the regeneration of multilevel codes.

1.2 Low-frequency components of B-code

Since with the B-code there are never more than 4 zeros or 4 ones in succession, the lowest frequency component which can have full amplitude is $f_0/8$, where f_0 is the pulse repetition frequency (bit rate). The contribution of any lower frequency component can be estimated by assuming a pulse-train of the form

.... 1010*1111*0101 .... 0101*0000*1010 .... 1010*1111*0101 ...

with any number of 01's or 10's between the blocks of 4 ones or 4 zeros. Neglecting the contribution of the 01 series, it is found that the maximum relative values of the Fourier coefficients are approximately equal to $\sin(af/f_0)$, where $a = 4\pi$. For example, the maximum component at $f = f_0/100$ is 0.125 A_0 or 18 db down, compared to the component of $f = f_0/8$, and all the components below that frequency will be still smaller in proportion to the frequency. (The value of A_0 depends on the length of the pulses compared with the pulse spacing. For rectangular pulses of maximum length $A_0 = 4/\pi = 1.27$ times the pulse height.)

1.3 Coding

Most of the coders used for binary systems can be adapted to produce the A-code. Take, for example, the serial coders described by *Villars* [1][1]) or *Gibbons* [2]. Here the weights of the digits are

1, 2, 4, 8, 16, 32, etc.

If these weights are changed to

1, 1, 3, 3, 9, 9, 27, 27, etc.

and all the even digits are inverted, we obtain directly the A-code. Actually, this arrangement is to be preferred for telephone coding for the following reason. In a binary code

[1]) Refer to the Bibliography at the end of the article.

the most critical transition occurs in the centre of the amplitude range, that is at the zero crossing of the input signal. In the case of a 7-digit code, for example, this is represented as the transition between the numbers 63 and 64, whereby 64 is the weighted output of the first digit, whereas 63 is obtained as the sum of the other 6 digit outputs,

$$32 + 16 + 8 + 4 + 2 + 1 = 63$$

The summing operation is usually performed by means of a resistor network and transistor or diode switches. Any inaccuracy in the components involved results in an inaccuracy or even an error in this step, just at the point where it is most noticeable in a telephone system. With the ternary code, on the other hand, these critical transitions occur at one third of the total amplitude range, which means that they can only affect relatively loud voice signals.

In addition to the usual types of coders there is a parallel coder to be described later, which takes advantage of the peculiar periodicity of a certain type of unit distance code called the C-code, which can be converted into the A-code.

1.4 Multiplexing

If a large number of voice channels is to be combined in a PCM system, the most appropriate form of multiplexing is by time-division. Multiplexing can be done either before or after coding. However, it is usually not economical to code each channel separately, and not practical to code a large number of them (say 1000) in a single coder. Therefore, the trend is towards relatively small groups of channels (say 25) which are combined by PAM multiplexing and coded in a common coder. The resulting pulse pattern will be as shown in Fig. 1a. All the digits belonging to a particular character are grouped together, and one can balance the code as explained above.

If now several of these groups are to be combined to form a larger system, the easiest way would be to interlace the pulse trains belonging to the various groups as shown in Fig. 1b. However, this would mean that there were rows of digits which belonged to independent groups and therefore could all be zeros or all ones, and most of the advantages of the balanced code would be lost.

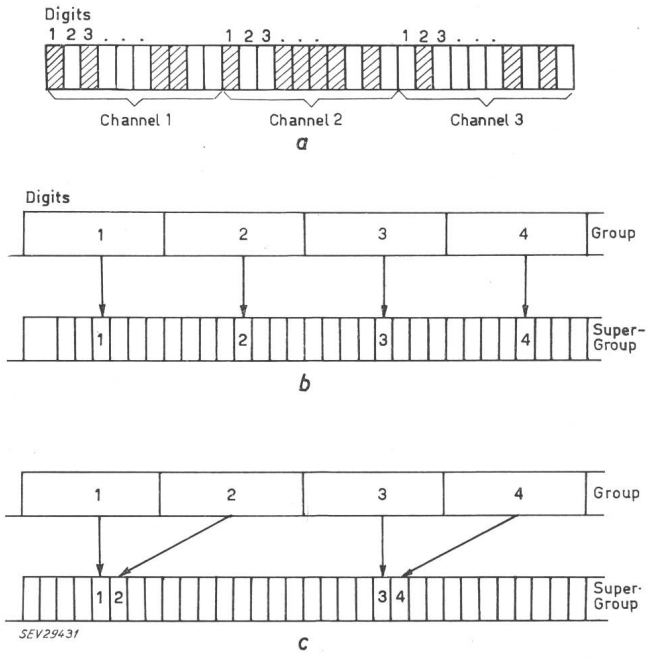


Fig. 1

Time-multiplexing of telephone channels

a Group pattern; *b* Conventional multiplexing; *c* A-code multiplexing

This can be avoided with the multiplexing scheme shown in Fig. 1c where pairs of digits are left together. If one starts off with an A-code in each group, the resulting pattern will then still be an A-code which can be transformed in the normal way into a B-code.

One method to obtain the pattern of Fig. 1c is to separate even and odd digits in each group onto two different lines, and delay one of them until the two digits of each pair are in time coincidence. Then, the two lines are separately multiplexed with the corresponding ones of other groups; finally the two resulting pulse-trains are interlaced again.

Another method is to do the multiplexing with the signals in ternary form (3-level), in which case only one line per group is required. Symmetrical transistors may be useful for the gates in this case.

1.5 Data transmission and electronic switching

It is suggested that data signals might be handled in ternary form, with two of the three levels carrying the binary information; the third level being used to provide synchronizing or framing pulses.

Either the A-code or the ternary code could be used in electronic exchanges with time-division switching. They would be converted into the B-code before being sent onto an outgoing line. Incidentally, this has the advantage that there is always a balanced signal on the line, even if the input to the converter is open-circuited. This is necessary to ensure that the regenerators along the line are always receiving timing information.

1.6 Code conversion

It was said that the various codes discussed in this paper can all be transformed into each other. It will now be shown by means of conversion tables how this is done. The tables contain code tables, transformation functions in Boolean algebra, and logic circuit diagrams. There is usually more than one solution, and the example given in each case should be regarded as representing one out of several possibilities, and not necessarily the best one, this being dependent on the type of circuitry employed.

If odd and even digits of an A-code are separated, as explained above, the odd digits are denoted by A_1 and the even digits by A_2; and similarly for the other codes. The inverse of A is denoted by $\overline{A}$. The type of gates used in the circuits are indicated by a number, say n, which means that the output is equal to 1 only if n or more inputs are 1. For example,

the number 1 denotes an OR-gate,
2, if there are only 2 inputs, an AND-gate.

The following code conversions are given:

Table 2: A to B-code

Here, F(x) is defined as that function of x which changes from 0 to 1 or from 1 to 0 whenever x changes from 0 to 1.

A- to B-code conversion Table II

a) Table

A_1	A_2	B_1	B_2			
0	1	0	1			
0	0	0	0	or	1	1, alternating
1	0	1	0			

b) Functions

$B_1 = A_1 + x\mathrm{F}(x)$ $\quad x = \overline{A_1}\,\overline{A_2}$ $\quad A_1 = B_1\,\overline{B_2}$

$B_2 = A_2 + x\mathrm{F}(x)$ $\quad\quad\quad A_2 = \overline{B_1}\,B_2$

c) Circuits

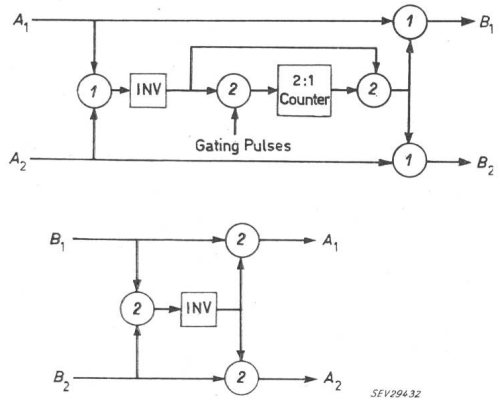


Table 3: Ternary to A-code

This cannot be expressed in Boolean algebra but is so simple that it will be evident from the figure.

Ternary to A-code conversion Table III

a) Table

Ternary	A_1	A_2
0	0	1
1	0	0
2	1	0

b) Waveform

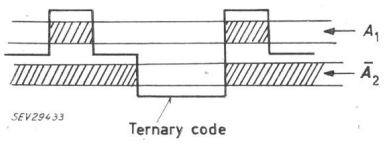


Table 4: C to A-code

This transformation will be explained in connection with the parallel coder.

Table 5: Binary to A-code

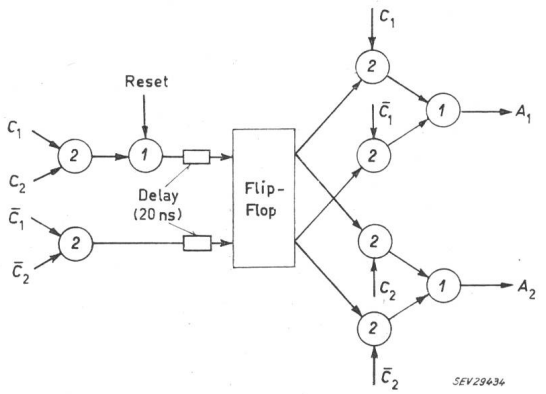
It will sometimes be necessary to transmit information given in the usual binary form over a system which accepts only balanced codes. The simplest way to do this is to use two digits of the A-code for each binary digit, as explained for data signals. A more economical, although more complicated way, is shown in this table. 3 binary digits are represented by 4 digits of the A-code. This is possible because there are 9 characters available in the latter, and only 8 are required for the former.

C- to A-code conversion Table IV

a) Table

The conversion table is given in graphical form in Fig. 4

b) Circuit



Binary to A-code conversion Table V

a) Table

binary			A-code			
a_1	a_2	a_3	A_1	A_2	A_3	A_4
0	0	0	0	1	0	1
0	0	1	0	1	1	0
0	1	0	1	0	0	1
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	1	0	1	0	0
1	1	0	1	0	0	0
1	1	1	0	0	1	0

b) Functions

$a_1 = \overline{A_1}\,\overline{A_2} + \overline{A_3}\,\overline{A_4}$ $\quad A_1 = \overline{a_1}\,a_2 + a_2\,\overline{a_3}$

$a_2 = A_1 + a_1\,A_3$ $\quad A_2 = \overline{a_1}\,\overline{a_2} + \overline{a_2}\,a_3$

$a_3 = A_3 + a_1\,A_4$ $\quad A_3 = \overline{a_1}\,a_3 + a_2\,a_3$

$A_4 = \overline{a_1}\,\overline{a_2} + \overline{a_2}\,\overline{a_3}$

2. Parallel Coder for Television

2.1 Introduction

A parallel coder is one in which all the digits belonging to a sample appear simultaneously on parallel wires, whereas in a serial coder they appear one after the other on a single line. A parallel coder followed by a parallel-to-serial converter was considered to be more suitable for television because its main circuits work at a lower frequency.

The aim was to develop a solid-state coder for TV However, since suitable transistors were not obtainable at that time, the first model was built using valves and diodes. This coder works at a sampling rate of 10 Mc/s and a final pulse rate of 100 Mc/s. Only 7 out of the available 10 digits are used producing $2 \times 3^3 = 54$ levels. Then, a transistor model of the main part of the coder working at low speed was built. This produces an 8-digit 81-level code and is used mainly to study the principles of this type of coder. The next step would be to build the same coder with faster transistors for a sampling rate of 12.5 Mc/s and a pulse rate of 100 Mc/s.

2.2 *Choice of standards*

Each sample of the video waveform represents one spot of the television picture. For equal horizontal and vertical resolution and an aspect ratio of 4/3, the number of spots per line should be equal to 4/3 times the number of lines per picture. In practice, the available vertical resolution cannot be fully utilized because of interlace flicker. Therefore, it is permissible to use a somewhat smaller number of spots per line. However, one should not go too far in this direction, since future TV receivers may have some means of storage between frames to reduce interlace flicker.

About 18% of each line is lost for the synchronizing pulse and black porches, and 8% of the number of lines is lost for the frame synchronizing signals. If this is taken into account, the sampling frequencies given in Table 6 are obtained for the four existing TV systems, assuming equal horizontal and vertical resolution.

Sampling frequencies

Table VI

System lines	Line frequency kc/s	Sampling frequency Mc/s
405	10.125	6.2
525	15.750	12.3
625	15.625	14.6
819	20.475	24

It appears from this table that 12.5 Mc/s would be a good choice as a standard sampling frequency. It provides 100% resolution for a 525-line picture and 85% resolution for a 625-line picture. This is expected to give about the same overall quality for the two pictures, considering the lower flicker frequency of the 625-line picture. Two 405-line pictures can be combined by time division multiplex to be transmitted over the same channel. An 819-line picture, on the other hand, can be split up into two channels of 12.5 Mc/s sampling speed such that even samples are transmitted over one channel and odd samples over the other channel. It is one of the advantages of a PCM system that combinations like these can be made comparatively easily (after coding).

An 8-digit B-code provides for 81 amplitude levels to represent the brilliance of each spot. This in itself is not considered to be quite adequate for a good TV picture. However, one can make use of the fact that a higher number of levels is required only for the reproduction of picture areas which extend over many spots, and not for each individual spot. For this purpose, one half of a level is added to each second sample before coding. The effect is shown in Fig. 2. In the transition region between two levels the resulting video waveform is alternating between the upper and lower level, creating the impression of an intermediate shade of gray. A further refinement of this "level interpolation" method is obtained if the decoder produces the mean value of a sample and the previous one, whenever they differ by one level only. The effective number of levels for frequencies below one quarter of the sampling frequency is thereby doubled.

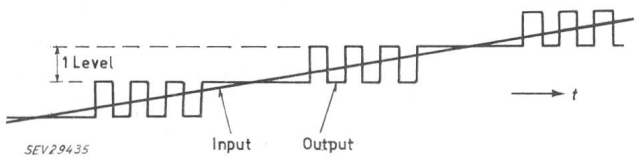


Fig. 2

"Level interpolation" improves the effective amplitude resolution for low frequencies

With this improvement, an 8-digit 81-level code is expected to be adequate for the reproduction of a good quality picture. More practical tests are required, however, to confirm this. With a sampling frequency of 12.5 Mc/s it would lead to a total bit-rate of 100 Mc/s, or a time-interval of 10 ns available for each digit.

2.3 *Basic circuit*

In principle, the coder contains one amplitude-discriminator for each transition between adjacent levels. However, since it is not practical to connect 80 amplitude-discriminators in parallel, the total range of amplitudes is first subdivided into a number of smaller ranges by means of the "group separator" shown in Fig. 3. The signal current I, representing the TV waveform, is supplied from a high-impedance source through point A to a number of diode discriminators. The latter consist of two diodes D_1 and D_2 and a resistor R_1. The outputs $B_1 \ldots B_m$ are held at fixed potentials, separated by E_d which is of the order of 1 V. For the purpose of this discussion the currents I_1 supplied through R_1, and I_2 supplied through R_2, are assumed to be constant. Transistors are assumed to be of the npn-type, but obviously they can be replaced by valves or pnp-transistors if the supply voltages are chosen accordingly.

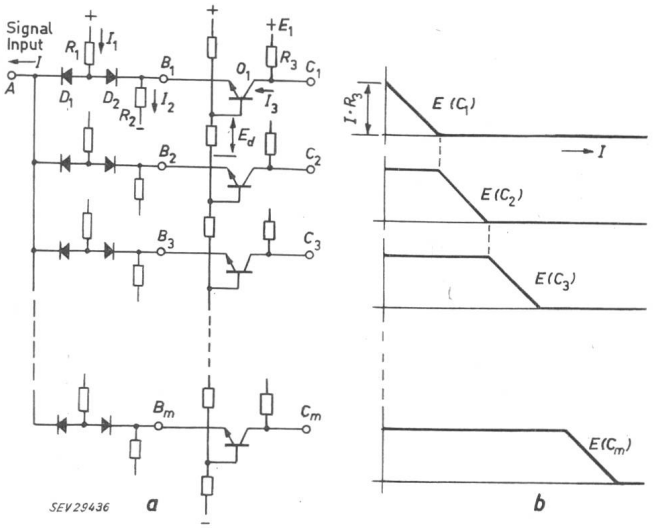


Fig. 3

"Group separator" for dividing the amplitude range into groups of 6 or 12 levels

a Circuit; *b* Voltages at points C_r ($r = 1 \ldots m$)

If $I = 0$, all the diodes D_1 are non-conducting and I_1 flows through D_2. Therefore $I_3 = I_2 - I_1$, neglecting the base current of the transistor. If I now increases from zero, part of I_1 is diverted through D_1 in the most positive discriminator, and the output current will rise proportionately,

$$I_3 = I_2 - I_1 + I$$

until $I = I_1$, when I_3 will remain equal to I_2. The resulting voltage $E(C_1)$ at the output C_1 as a function of input current I is shown in Fig. 3b.

For $I > I_1$ the second discriminator comes into operation until $I = 2\ I_1$ and so on until the maximum $I = mI_1$ is reached. Each of the output voltages $E(C_1)$ to $E(C_m)$ has a linear portion representing a part of the total amplitude range of the TV signal. Each output C_r ($r = 1...m$) will be connected to a "coder subunit" dealing with k level-transitions, and since there are m of these, a total of $mk + 1$ levels are available.

In a parallel coder it is preferable to make use of a "unit-distance code" in which only one digit changes at each level-transition. The "C-code"[2]) shown in Fig. 4 has this property and in addition it can be transformed relatively easily into the A-code as will be explained later.

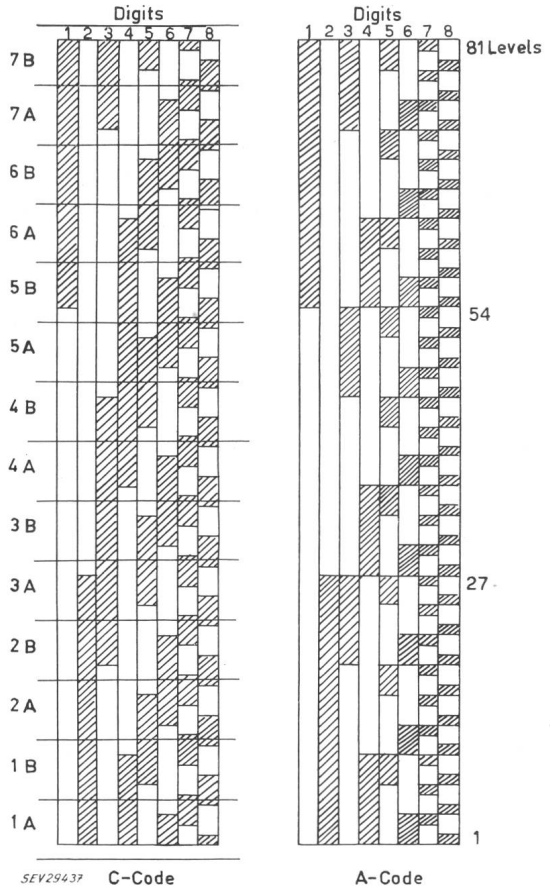


Fig. 4
81-level C- and A-codes
▭ = 0 ▨ = 1

The last two digits of this code have a periodicity of 6 levels. Therefore, it is appropriate to choose $k = 6$ or $k = 12$.

A circuit of a 6-level coder subunit is shown in Fig. 5c. Its operation will be explained by reference to Figs. 5a and 5b. The input C_r is connected to one of the outputs $C_1...C_m$ of the group separator (Fig. 3). The two transistors Q_2 and Q_3 form a "long-tailed pair" and produce two outputs of opposite phase at the collectors. Resistors R_6 and R_7 are used to shift the DC-component of these voltages. R_6 and R_7 are small compared to R_8. Therefore, the voltage drops across R_6 or R_7 can be assumed to be constant in a first approximation. The relative potentials at the six points $a...f$ will then vary as a function of input current I as shown in Fig. 5b and they will pass through a fixed potential E_W one after the other at equally spaced intervals. These six crosspoints will represent the six level-transitions of the coder subunit. For this purpose, the circuit of Fig. 5c is used. The three diodes connected to a, d and x form an AND-gate. If and only if both a and d are more positive than E_W, a current determined by R_9 will flow through R_W and produce a positive output voltage at x. This is indicated in Fig. 5b. The output z will behave in a similar way, except that the on-interval is shifted by two levels to the right, that is to higher input current I. The output y would follow the dotted line in Fig. 5b if b and b' in Fig. 5c were joined together.

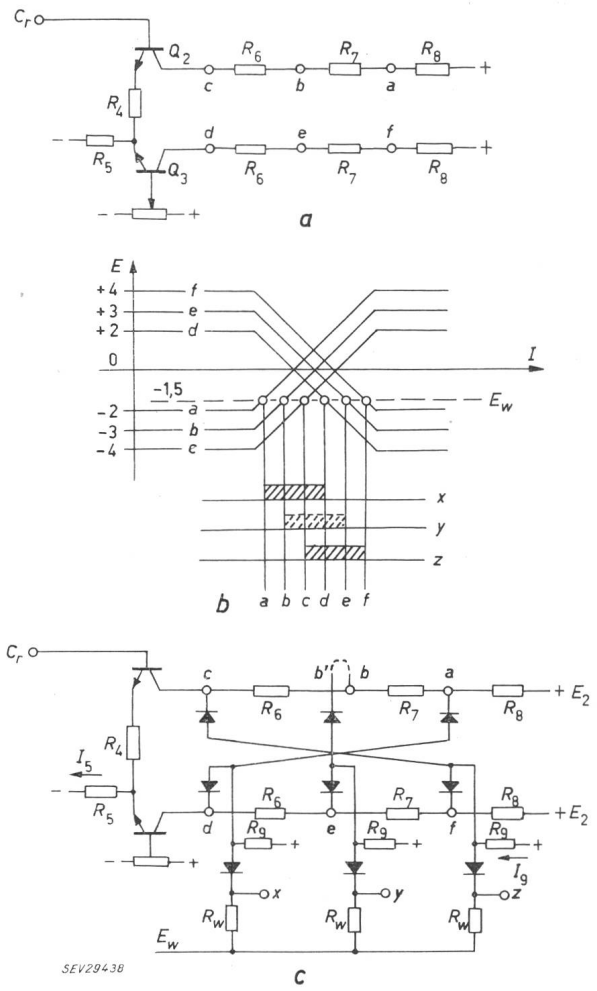


Fig. 5
"Coder subunit" for 6 levels
a Basic circuit; *b* Voltage E at the points $a...f$ as a function of input current I; *c* Coder subunit; E_w Transition voltage

In the complete coder, the outputs x from all the subunits are joined together, with a common load resistor R_W, and so are the outputs z. The resulting patterns of both x and z will be: 3 levels on, 3 levels off, as required for digits 7 and 8 of the C-code. Actually, the inverse of x is made to represent digit 7, and the inverse of z is made to represent digit 8. This will be apparent from the code-pattern of Fig. 4 where the ranges of the various subunits are denoted by 1A, 1B, 2A, 2B, etc. and the signal current I is assumed to be increasing towards the top.

[2]) This code was first suggested by *K. W. Cattermole*.

The first six digits can be obtained from combinations of the outputs y, if the terminals b and b' are suitably interconnected between the subunits. For example, b in subunit 2A is connected to b' in 2B, and y in 2B to digit 6. This turns digit 6 on for all the levels from 10 to 21. Similarly, if by going from a lower to a higher level, a particular digit is found to be turned on in one subunit and off in another, b of the first must be connected to b' of the second, and y of the second to the particular digit. In this way the whole code pattern is produced, except the top parts of digits 1, 3 and 5. To obtain these, the b's of subunits 5B, 7A and 7B have to be connected to three separate diode gates. They contain two diodes only and the outputs, which are similar to y outputs, are connected to the three digits mentioned. b' of subunits 1A, 1B and 3A are not used.

It may be noted that digits 1 to 6 come out direct whereas 7 and 8 are inverted. This is because in the C-code the sequence of digit-transitions is

on — off — on — off — on — off ...

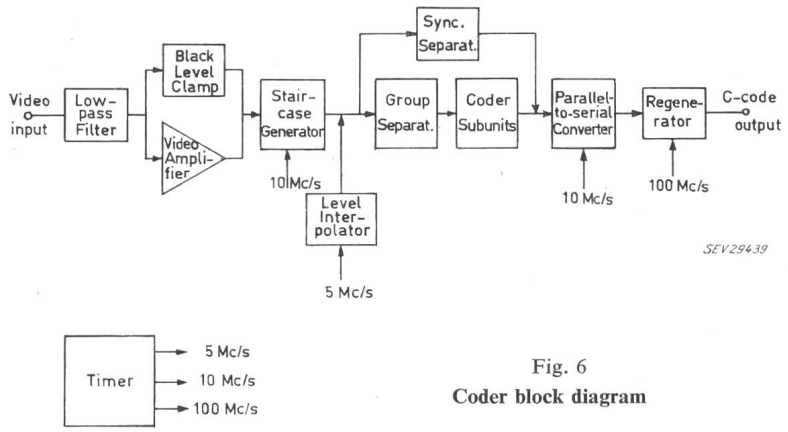


Fig. 6
Coder block diagram

whereas in the coder it is

on — on — on — off — off — off ...

This latter property is one of the features which make this type of coder practical, because it allows all the subunits to be identical. It would not seem to be so easy if a reflected binary or *Gray* code were to be used.

The above circuit description was based on idealized assumptions. For a more accurate analysis the currents drawn from the diode gates into the points a to f have to be taken into account as well as the finite values of all the resistances, base currents of transistors and various minor imperfections of transistors and diodes. By a careful choice of operating conditions, the circuit can be made to be fairly insensitive to transistor and diode characteristics, relying chiefly on the accuracy of resistors and ratios of supply voltages.

2.4 A 54-level valve coder

A coder utilizing these principles has been built[3]). Only 54 levels, that is the lower two thirds of the C-code of Fig. 4, are provided. Therefore, the first digit can be omitted, leaving 7 active digits. The sampling rate is 10 Mc/s and the serial digit rate 100 Mc/s. There are 3 spare digits which are not used.

The block diagram is shown in Fig. 6. The incoming video signal passes through a low-pass filter, is amplified to a level of about 12 V peak-to-peak, and its black porch following the line synchronizing pulse is clamped to −160 V with respect to ground. The synchronizing pulses are positive and the picture negative at this point. A cathode follower is used to drive the "staircase generator" which samples the video waveform during 50 ns and holds the output constant for the next 50 ns (Fig. 7). This is to make sure that all the digits refer to the same amplitude level in case they have somewhat different delays until they are transformed into serial form.

The resulting waveform is applied to the grids of two pentodes type 6761 in parallel, which act as a current generator to drive the group separator. (Actually, these valves tend to be overloaded and should be replaced by more powerful ones or more of them in parallel.) A catching diode prevents the anodes from getting too positive with a resulting loss in speed in case of too large an input signal.

The circuits of Fig. 3 and Fig. 5 are used for the group separator and coder subunits, except that the transistors have been replaced by triodes type 417A. The following design values have been adopted:

$m = 9$	$R_3 = 680\ \Omega$
$I_1 = 10$ mA	$R_4 = 180\ \Omega$
$I_2 = 20$ mA	$R_5 = 2.9$ kΩ
$I_5 = 30$ mA	$R_6 = 82\ \Omega$
$E_1 = 100$ V	$R_7 = 68\ \Omega$
$E_2 = 250$ V	$R_8 = 1.5$ kΩ
$E_w = 224$ V	$R_9 = 13$ kΩ

Diodes: OA 79

The grounded grid valve corresponding to Q_1 in Fig. 3 has been transferred into the coder subunit in order to reduce wiring capacity on the anode. The input impedance on the cathode is approximately 50 ohms and can be used as a termination of a co-axial cable.

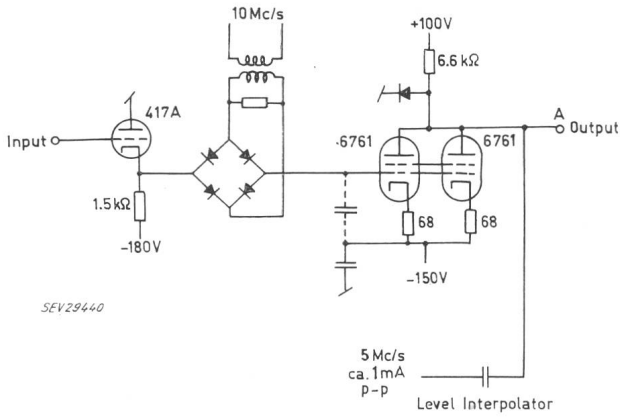


Fig. 7
Staircase generator and coder driving amplifier

The grid of this valve is connected to a voltage divider ranging from −21 to −37 V, each subunit receiving a different bias at intervals of $E_d = 2$ V. The interval was made rather large initially to make it uncritical with respect

[3]] The experimental work described in this paper was carried out by *D. E. Brown*'s group at Standard Telecommunication Laboratories Ltd., Harlow, Essex (England).

to diode and valve characteristics, but it was found that it could be reduced below 2 V with advantage.

The 9 subunits produce a code of 53 levels representing brightness values between white and black. The 54th level is reserved for the synchronizing pulses. The latter are separated from the signal and made to open a diode gate (similar to the ones in the coder subunits) whose output is connected to point x of the subunits. This makes the 6th digit (No. 7 in Fig. 4) zero, thereby changing the 53rd level into the 54th.

The outputs x, y, z of the subunits are connected to the 7 digit amplifiers as explained before. The first stage of a digit amplifier is a grounded-grid triode which has a low input impedance at a dc potential of nominally +224 V. In order to allow the digit amplifiers to be ac coupled, the outputs of the subunits are chopped at a rate of 10 Mc/s by means of an additional diode connected to each 3-diode-gate. The resulting 50 ns pulses are dc restored after being amplified to about 15 V peak. Unfortunately, there is some capacitive breakthrough of the 10 Mc/s gating wave, which must be neutralized. For this purpose an out-of-phase sine-wave is added through small capacitors to the respective digit amplifiers. The dc restorers used were not very satisfactory, but it was not considered worthwhile to spend much effort in improving them, because in the transistorized version the digit amplifiers would be dc coupled anyhow.

The 7 digit amplifiers are connected to the suppressor grids of gating valves type 6AS6, the last two digits being first inverted. The control grids, on the other hand, are switched on by pulses of somewhat less than 10 ns duration and 10 Mc/s repetition rate. The anodes are connected to tappings of a delay line at intervals of 10 ns. The delay line is of the constant resistance type designed by *A. Russen* (Fig. 8). Its output represents the serial C-code of 7 digits.

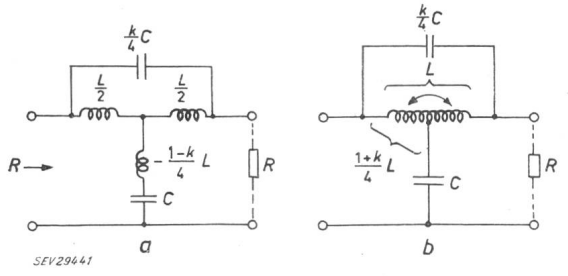


Fig. 8
Design of a constant resistance delay line
a Equivalent circuit; *b* Actual circuit

$$R = \sqrt{\frac{L}{C}} = \frac{2}{\sqrt{k'\,\omega_0\,C}} \qquad \omega_0 = \frac{2}{\sqrt{kLC}} \qquad L = \frac{4}{\omega_0^2\,kC}$$

Delay $T = \sqrt{LC} = RC$ (at $\omega = 0$)
$k = 1/3$ for maximally flat delay
$k = 0{,}4$ compromise value
2...4 sections per pulse

The remaining 3 digits can be switched on or off manually. Since there is some degradation of the pulses travelling down the line, they are regenerated at the end by means of the regenerator shown in Fig. 9. The transformers in this circuit have an input impedance of 200—600 Ω, an output impedance of 50 Ω and a frequency range of 0,2 to 100 Mc/s.

The C-code is of the "unit-disparity" type, which means that the numbers of ones or zeros contained in each character can change by one unit only. Thus, the 7-digit code produced by this coder has either 3 or 4 ones. Therefore, it is nearly "balanced" and it can be handled by ac coupled amplifiers and regenerators without the need for dc restoration, although it will not be as good as the B-code in this respect.

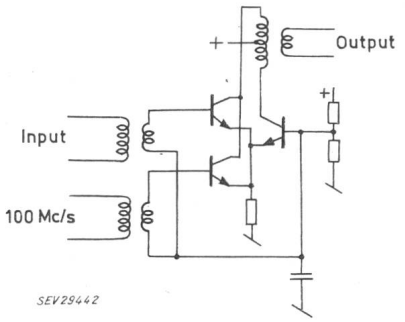


Fig. 9
Pulse regenerator (slicer and retimer)

In the first experiments, the C-code was actually used for transmission and at the terminal receiver it was decoded directly by means of diode matrices. However, this decoder was not very satisfactory due to spurious signals caused by diode capacity and hole storage effects. Therefore, it is suggested that the C-code should be transformed into the A-code and then into the B-code at the transmitting end. This would have the following advantages:

a) The B-code is a fully balanced code.

b) The maximum error caused by a false digit is 27 levels as compared to 54 levels with the C-code. This applies to both the 54 and 81-level codes.

c) Decoding is simpler, being done by weighted addition of the parallel digits. This is an advantage because there are likely to be more decoders than coders in a television network.

In spite of its many imperfections, the coder described above produced a fairly good TV picture, which most people could only with difficulty distinguish from the original. It must be noted, however, that the picture available for the tests was relatively noisy to start with, being received from the B.B.C. through an ordinary home-receiver.

2.5 An 81-level low-speed transistor coder

Transistors are inherently more suitable than valves for this type of coder because of their low base-to-emitter voltage compared to the grid-to-cathode voltage of valves. However, one is more likely to be limited by high-frequency cut off, maximum voltage ratings and power dissipation. Since the switching elements are semiconductor diodes, there is a lower limit on the voltage swings required for each switching operation. Coupled with the inevitable component and wiring capacities, this also puts a lower limit on the current levels ($C\,dE = I\,dt$).

In order to study the behaviour of transistors in these circuits, a low-speed model of the coder has been built. It is based on the same principles as the valve coder, but contains a few minor modifications. The number of levels has been increased to 81.

The circuit of Fig. 5c has one disadvantage. For low values of I (to the left of the transition region in Fig. 5b) the diode gate between a, d and x is supposed to be held off by the negative voltage at point a, which is only 0.5 V below E_W. If the diodes have unequal characteristics and the resistors are not very accurate, it can happen that some current is still flowing through the resistor R_W. This will persist throughout the range of levels below that point. If it occurs in more than one subunit, the currents add up and may simulate a false digit output in the end. It can be avoided if the diode gates are connected between the points d, e, f of one subunit and a, b, c of the next one, and the polarity of the diodes is changed at the same time. This is shown in Fig. 10. The gates are now held off by comparatively large positive voltages. The difficulty of marginal switching can still arise in the on-state, but this is limited to the range within one subunit and is not cumulative. On the other hand, the circuit has the disadvantage that more interconnections between the subunits are required.

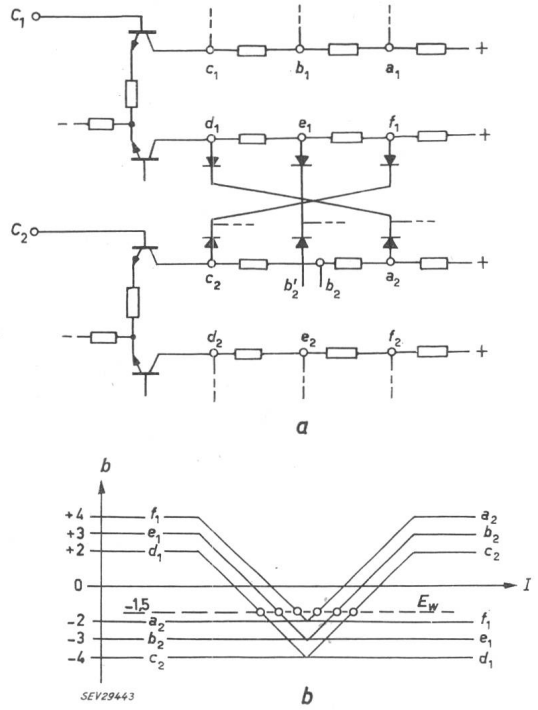


Fig. 10

Alternative interconnection of subunits to reduce spurious outputs

a Circuit; *b* Voltage E at points $a \ldots f$ as a function of input current I; E_w Transition voltage

An 81-level coder would require 14 subunits of 6 levels and the group separator would consist of 14 diode gates in parallel. This means a rather high capacitive loading and a large voltage swing at the input, which is undesirable. Therefore, two subunits have been combined into one as shown in Fig. 11a. The two halves are denoted by A and B which corresponds to the group notation of the code in Fig. 4. An alternative method is shown in Fig. 11b, which is only applicable, however, if the transistors can stand a reverse base-to-emitter voltage of a few volts.

Actually, the transistors used for this low speed coder were of the pnp-type, which means that the polarities of all the diodes and supply voltages had to be reversed.

The values were chosen as follows:

$I_1 = 1.7$ mA	$E_d = 1$ V	$R_4 = 2.5$ kΩ
$I_2 = -0.3$ mA	$E_1 = -28$ V	$R_6 = 680$ Ω
$I_5 = 2$ mA	$E_2 = -50$ V	$R_7 = 560$ Ω
$I_9 = 0.1$ mA	$E_w = -38.4$ V	$R_8 = 7.5$ kΩ
	$E_A = -27$ V	$R_9 = 390$ kΩ
	$E_B = -24$ V	$R_{10} = 5.1$ kΩ
	Transistors: 2 N 247	
	Diodes: OA 266	

In the group separator the resistors R_1 have been replaced by transistors with current feedback to obtain a higher impedance at a low supply voltage.

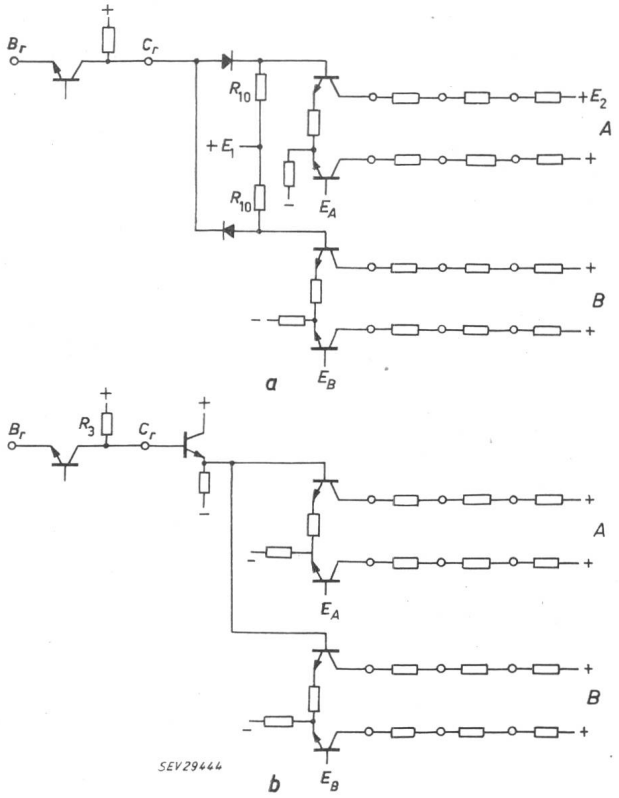


Fig. 11

Double subunits for 12 levels

a, *b* Alternative methods

The supply voltages indicated are approximate only and have to be adjusted for best results.

The subunits are wired by means of solderless wrapped connections, whereby the terminal and component wire are put together and another wire wrapped around the two (secondary wrapping). Terminals are of the U-link type, fixed to the board by the wrapping only. The subunits are also interconnected by wrapped wiring rather than plug-in connectors. This has the disadvantage that servicing is rather awkward, but the advantage of reduced wiring capacitance. It is expected that the same construction could be used for a full-speed TV coder.

Discussion of Results

Although the two coders described above were designed for equally spaced amplitude levels, in practice the steps were somewhat unequal. In particular, each 6th step, representing the transition from one subunit to another, is likely to be bigger than the other 5 steps. It can be avoided by careful adjustment, but then the circuit becomes more sensitive to component changes.

The result of this non-linearity on the overall characteristics of the system, assuming an ideal decoder, is shown in Fig. 13a. Fortunately, in a television picture, this type of distortion can hardly be noticed. The important thing is

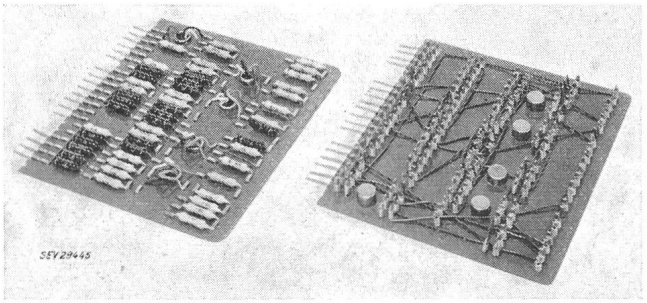


Fig. 12
A double subunit wired with wrapped connections

that the height of each step does not exceed a certain limit and this is what determines the total number of levels required. The inverse distortion as shown in Fig. 13b, therefore, would seriously degrade the picture. Thus, a coder with a somewhat unequal distribution of levels can be tolerated as long as the decoder produces fairly uniform steps, which is not so difficult to achieve.

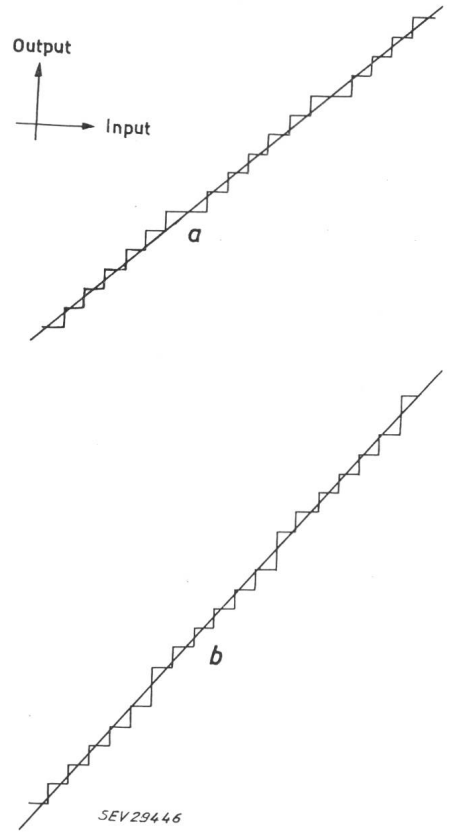


Fig. 13
Distortion caused by unequal spacing of levels
a Coder non-linear, decoder linear
b Coder linear, decoder non-linear

Point-contact germanium diodes have been used in the experiments. So far, junction types did not seem to be suitable, unfortunately. This appears to be due to the fact that the circuits are mainly of the current switching type, with little reverse drive being available to remove stored charges. It might be improved somewhat by changing towards voltage switching, but this would make it more dependent on diode characteristics.

Recently, transistors have become available which should allow an all-solid-state coder to be built, with the possible exception of the driving amplifier. Some of the transistor types to be considered are, for example,

2 N 706, 2 N 697, 2 S 101

Code-Converter and Decoder

The C-code produced by the coder can either be transformed into the A-code while it is still in parallel form, or the odd and even digits can first be serialized separately and then transformed. The latter method is more economical in the number of transistors and will be described here. It should be noted that the circuits of this section have not been built but are given as suggestions only.

It is assumed that an 8-digit code with a sampling rate of 12.5 Mc/s is used. The four odd digits are converted into serial form with digit No. 1 being first in time and the others following at 20 ns intervals. Similarly, the four even digits are serialized, digit 2 being in time coincidence with digit 1. The two resulting signals will be denoted by C_1 and C_2 respectively. Each of these has to pass one or more trigger stages in order to assure that each digit will be definitely in one or the other state. The C-code can then be converted into the A-code and the B-code by means of the logic circuits given in Table 4 and Table 2 of Chapter 1. The flip-flop in the C-to-A converter has to be reset to the same state at the beginning of each 8-digit cycle.

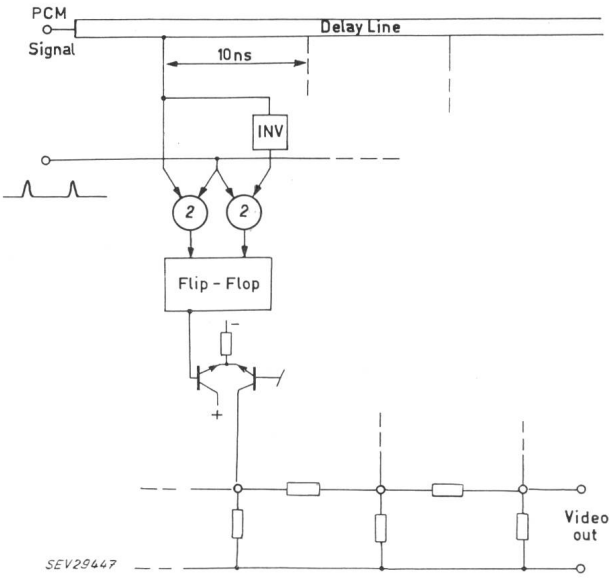


Fig. 14
Decoder for A- or B-codes

In the end, B_1 and B_2 are interlaced to form the final serial B-code with 100 Mc pulse rate.

The decoder contains a serial-to-parallel converter and a resistive combining network (Fig. 14). The long-tailed pairs, which are used to switch specified amounts of current into the network, are fed from different sides of the flip-flops for odd and even digits respectively. This is because

the output currents are of one polarity only whereas the code is essentially symmetrical. The decoder accepts either A-or B-codes without change.

Synchronization

In the normal TV signal, the line synchronizing pulses take up about one quarter of the amplitude range, but only one character of the code is required to represent them. Therefore, in the coder, the synchronizing pulses are separated

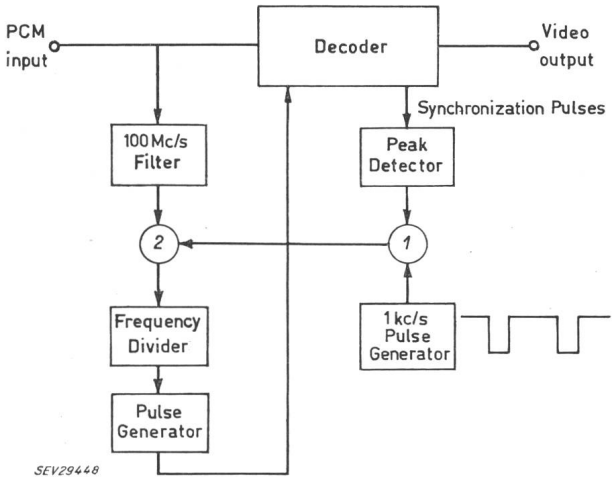


Fig. 15
Synchronizer

from the signal as explained above for the 54-level coder. In the decoder, this character is recognized separately and made to feed the required amount of current into the combining network.

Incidentally, this method also makes possible a relatively simple means of synchronizing the decoder. Here, the problem is to find out which is the first digit of each character of the incoming pulse train. It was solved by the system shown in Fig. 15. A 100 Mc/s timing wave extracted from the signal is fed through a gate to a frequency divider which in turn controls the serial-to-parallel converter in the decoder. The gate is closed periodically by a free-running oscillator producing 1 kc/s pulses. Since these pulses are in no way correlated to the 100 Mc/s wave, the frequency divider starts fresh after each pulse and the phase of the divided frequency will change according to some statistical distribution. As soon as the phase is right, however, the decoder will produce the line synchronizing pulses and these will disconnect the 1 kc/s oscillator, so that the frequency divider will now stay in its correct phase.

With the 81-level code, the characters representing the top or bottom levels are not suitable for this purpose because of their periodic structure. However, this can easily be changed by inter-changing two digits, say, digits 7 and 8 (throughout the system).

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[2] *P. L. W. Gibbons:* The Application of Transistors to Digital Speech Communication Systems. IEE, International Convention on Transistors and Associated Semiconductor Devices, May 1959, Paper No. 2983.

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Réalisation et performance des codeurs binaires hyperboliques

Par *C. P. Villars*, Bienne

621.376.56 : 621.391

1° Introduction

Pour réaliser des vitesses de codage élevées de — 0,1 à 1 μs par bit et une bonne précision — de 6 à 10 bits — les codeurs binaires par rétro-action («Feedback Coding») [1][1]) sont particulièrement intéressants. Ces convertisseurs de signaux analogiques en expressions binaires codent un bit par opération du circuit. Ils sont donc, du point de vue de la vitesse de codage, intermédiaires entre les codeurs à compteurs binaires [2] et ceux à tube cathodique («Beam Coding Tube») [3].

Considéré comme un système à réaction le codeur (fig. 1) se décompose en un circuit direct et un circuit de réaction. Le circuit direct est formé par un comparateur qui peut être décrit par les relations suivantes:

$$e_2 = 1 \text{ pour } e_1 > 0$$
$$e_2 = 0 \text{ pour } e_1 \leqq 0 \qquad (1)$$

Idéalement sa caractéristique est une marche d'escalier. En pratique, on réalise un amplificateur ayant un gain très grand et très stable pour les valeurs du signal autour de zéro et un gain fortement limité dès que le signal a une amplitude suffisamment grande, soit positive, soit négative. Le circuit de réaction — béta — est un décodeur qui transforme l'information binaire en une grandeur analogique. Celle-ci est comparée au signal d'entrée au moyen d'un circuit d'addition. Le système travaille donc comme un

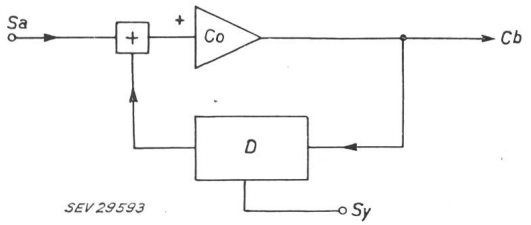

Fig. 1
Schéma général d'un codeur à rétro-action
Sa Signal analogique; *Co* Comparateur; *Cb* Code binaire; *D* Décodeur; *Sy* Synchronisation

servo-mécanisme. Il va tendre à minimiser l'erreur à l'entrée du comparateur. En d'autres termes, le signal du décodeur devient égal au signal d'entrée avec une précision égale à $\pm \frac{1}{2}$ quantum de résolution.

[1]) Voir bibliographie à la fin de l'article.