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Autor(en): **Therez, F. / Silva, M. da**

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# Two-Dimensional Channel from $Ga_{0.65}Al_{0.35}As$-GaAs undoped heterojunction

F. Therez and M. Da Silva
LAAS-CNRS, 7, Av. du Colonel Roche, F-31077 Toulouse (France)

**Abstract.** We have designed structures of the high-mobility channel induced at the interface of a $Ga_{0.65}Al_{0.35}$ As insulator and an undoped GaAs heterojunction. The $Ga_{0.65}Al_{0.35}$ As layer is located between the N-type GaAs at the bottom of the heterostructure and the undoped GaAs region on the top of the device. The high-mobility of the electron density in the channel is induced by positively biased the N-type GaAs layer. The measured results have demonstrated that the two dimensional channel is controlled by the gate voltage. We detail the conduction mechanism in the channel and the on-resistance value.

## I) Design and physical behaviour of the structure

The structure is based on an undoped GaAs and a N-type GaAs layers separated by the potential barrier made from $Ga_{0.65}Al_{0.35}As$ non intentionally doped material. The structure cross-section is shown in fig. 1 ; the widths of the undoped GaAs and GaAlAs layers are about 0.22 micron.

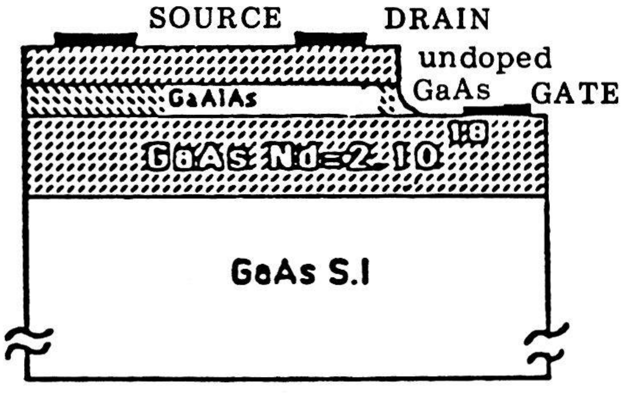


Fig. 1 Structure cross-section.

The N-type GaAs conducting region is taken to be 0.9 micron thick. At equilibrium the top undoped GaAs layer and GaAlAs insulator are depleted by the surface potential. The study of the circuit's parts corresponds to the design as follows. The source and drain electrodes are on the GaAs undoped layer. The gate contact is made on the N-GaAs buried region. Fig. 2 gives the energy band diagram when a positive voltage $V_G$ relative to the source is applied to the buried gate.

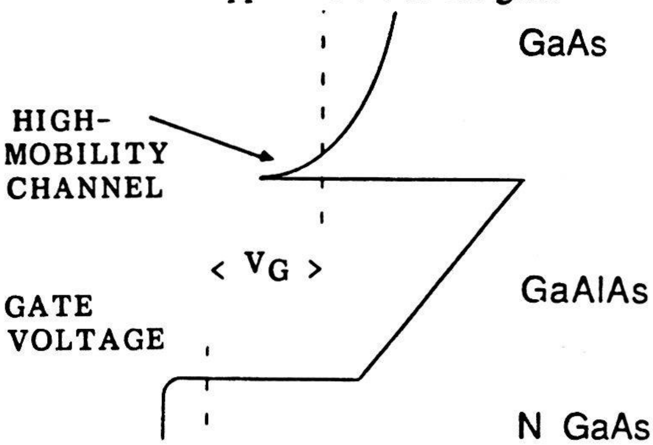


Fig. 2 Energy band diagram when a buried gate voltage $V_G$ is applied.

Under this condition, the upper interface is put below the Fermi level and a high mobility electron channel is induced. The channel is produced at the undoped heterointerface by the buried-gate action of the second conducting layer. Higher gate voltages enhance electron concentrations in the channel. Positive biases applied to the N-GaAs produces hot electrons in the channel at the undoped GaAs-GaAlAs interface. The rectangular GaAlAs potential barrier provides a better insulation between the two conducting layers. By applying $V_G$, the carriers are heated, resulting in thermionic emission currents across the potential barrier. In the charge injection case, the shape of the barrier is such that the reverse flux of electrons from the gate into the channel can be neglected.

The several layers were grown by organometallic chemical vapor deposition. The structure was grown on a (100) oriented semi-insulating GaAs substrate. The electron mobility was higher than 5000 $cm^2/V.sec$. The donor concentration of the N-GaAs was determined from C(V) measurement to be $2.10^{18}$ $cm^{-3}$. The Al mole fraction of the GaAlAs region was 0.35. The alloys for the source and the drain are made by evaporating AuGe-Ni. The undoped GaAs and $Ga_{0.65}Al_{0.35}As$ layers under the gate were etched respectively with $NH_4OH + H_2O_2$ and

FH solutions. AuGe-Ni metal was also used for the gate electrode. A critical step in manufacturing the structure is to provide ohmic contacts to the two dimensional channel while preserving the insulation from the N-GaAs layer. The metallic contacts were alloyed and the annealing at 430°C for 3 sec. have been found a good treatment.

**II - Electrical characteristics and conduction mechanisms in the channel**

Our experimental study corresponds to the current voltage curves of the gate-source heterojunction and the set of output characteristics $I_D(V_D)$. Fig. 3 shows the gate-to-source curve at T = 300°K. High blocking characteristic for both polarities are obtained.

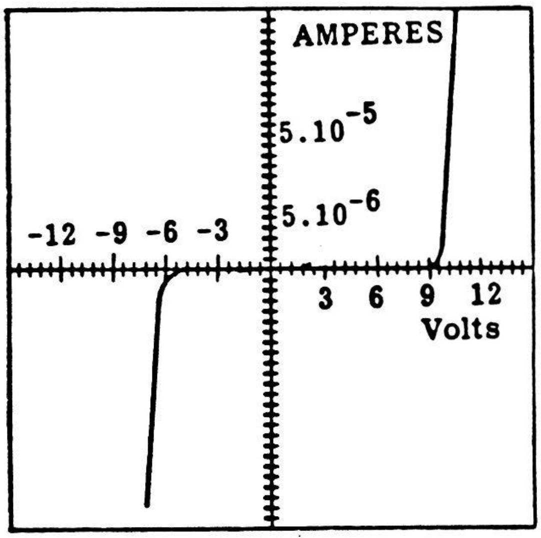


Fig. 3 - Gate-Source I(V) characteristic at T = 300°K

The turn-on voltages are about 9.5 and -5.4 volts. The $Ga_{0.65}Al_{0.35}As$ layer has good insulating results and gives an important reduction of parasitic leakage currents. For voltages higher than the turn-on points, the gate current increases rapidly and it is controlled by the thermoionic emission on the GaAlAs potential barrier.

Fig. 4 gives the source-drain $I_D$ ($V_D$) characteristics for several $V_G$ voltages. The channel starts at the threshold value $V_G = V_T$ and at $V_G$ higher than $V_T$ an important electron density is induced in the channel. Consequently high drain current is observed for positive gate voltages. The structure operates as a heterojunction field effect transistor, normally-off.

The high mobility electron channel decreases the access resistance. Generally the current crosses the GaAs and GaAlAs regions, these paths are shunted by the induced channel

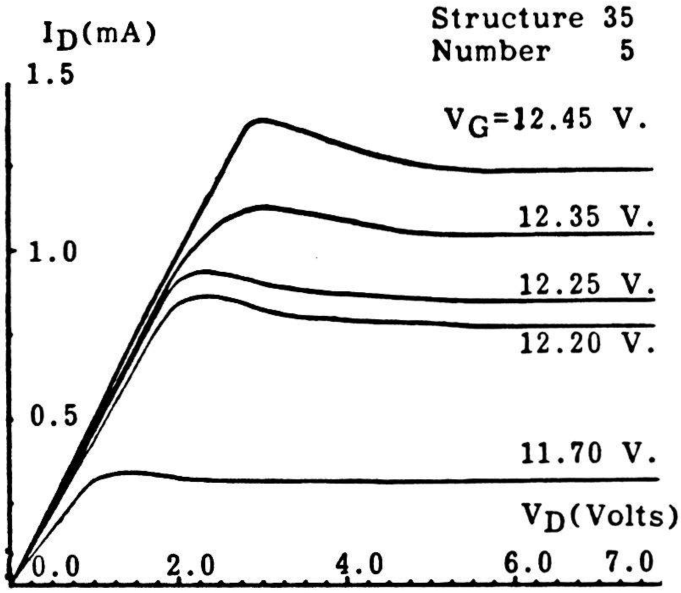


Fig. 4 - Output $I_D$ - $V_D$ characteristics for different $V_G$

resulting in a low value of the resistance at the source terminal. The ratio $V_D/I_D$ defines the contribution to the on-resistance and it is expressed as follows :

$$\frac{V_D}{I_D} = R_{access} + \frac{L.d}{\mu Z \varepsilon (V_G - V_T)} = R_{on}$$

where $\varepsilon$ and d are the dielectric constant and thickness of the GaAlAs layer. L and Z are the length and the width of the channel, $\mu$ its mobility. At small $V_D$ values, $R_{on}$ depends linearly on voltages $1/(V_G-V_T)$. The access resistance $R_{access}$ is given by the point where the line intercepts the vertical axis. We have characterized $R_{access}$ less than 15 ohms. We observe in Fig. 4 that carriers heated by the electric field applied parallel to the layer, from source to drain electrodes will move to the adjacent layers causing an enhancement of charge concentration in the N-GaAs layer and depletion in the channel. Finally, negative differential resistances are observed and the electrical behaviour may be explained by considering real space transfer electrons and energy transfer between the channel at the heterostructure and the N-GaAs layer.