Micropower Integrated Circuits

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MOS Analog Circuits

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Micropower Integrated Circuits

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Various aspects of the realization of micropower LSI circuits are discussed, from the requirements of CMOS technologies to constraints on systems. Available passive and active devices are reviewed, with emphasis on DC, AC and noise characteristics of transistors at very low currents. Problems and solutions encountered in digital and analog circuits are illustrated with some examples.

On examine les divers aspects de la réalisation de circuits intégrés à très faible consommation de puissance, depuis les exigences des technologies CMOS jusqu'aux contraintes sur les systèmes. Les composants actifs et passifs disponibles sont passés en revue, en insistant sur les caractéristiques et le bruit des transistors aux très faibles courants. Quelques exemples illustrent les problèmes et les solutions rencontrés dans les circuits digitaux et analogiques.

Verschiedene Aspekte der Herstellung von LSI-Schaltungen mit geringster Leistungsaufnahme werden besprochen, von den Forderungen der CMOS-Technologien bis zu den Ansprüchen der Systeme. Die verfügbaren aktiven und passiven Elemente werden durchgegangen und dabei insbesondere die DC-, AC- und Geräuscheigenschaften der Transistoren bei sehr schwachen Strömen betrachtet. Die in digitalen und analogen Schaltungen angetroffenen Probleme und Lösungen werden durch einige Beispiele illustriert.

1. Introduction

The power consumed for a given function in an integrated circuit must be reduced for either one of two different reasons. One reason is to reduce heat dissipation, in order to allow a larger density of functions on the chip. Any amount of power reduction is worthwhile, as long as it does not degrade the overall performance of the circuit. The other reason is to save energy in battery-operated instruments. This is mandatory in elctronic watches, where the average power available is only a few μW. Electronic watches have therefore been the driving force in the development of micropower ICs. Other existing or emerging applications are various kinds of pocket instruments, paging systems, implanted bio-medical devices, and devices for environment and security control.

Yet, some reduction in performance must be accepted to achieve micropower operation. The toll is usually a reduced speed for digital circuits and a reduced dynamic range for analog circuits. For practical reasons, voltage cannot be decreased below that of a single electrochemical cell, which is about 1.5 V. Most of the power reduction must therefore be obtained by reducing the current drain from the usual mA-level down to the μA-level or below. This brings about two important consequences:

1. Impedance levels are increased by more than three orders of magnitude, which increases the importance of leakage currents and parasitic conductances. Parasitic series resistances are generally negligible, and functional resistances cannot usually be implemented in a simple way.

2. Since the size of the components cannot be reduced, current densities are decreased by more than three orders of magnitude, which results in decreased speed of operation. Moreover, active devices may operate in an unusual range of their characteristics. This allows some new circuit schemes.

This paper will discuss technologies, devices, circuits and systems with respect to the realization of micropower LSI chips.

As the manuscript of the lecture on 'Micropower CMOS Analog Circuits' by E. A. Vittoz is not available, we present a paper on a similar subject by the same author, which was presented at the European Solid State Circuit Conference 1980 (ESSCIRC) in Grenoble. This paper is also published in NTZ Archiv 2/1982.

2. Technology

Although conventional bipolar [1; 2] or I^2L [3; 4] technologies may achieve interesting results in some specific applications, CMOS is unquestionably the best technology for micropower. The combination of dynamic and static power P consumed by a CMOS gate is roughly given by the well-known simple formula

$$P = f\,C\,V_B^2 + V_B\,I_0 \tag{1}$$

where f is the output frequency of the gate, V_B the supply voltage, C the output capacitance and I_0 the average leakage current.

Capacitance C is kept low by keeping substrate and p-well doping low ($1...5 \cdot 10^{15}$ cm^{-3}). Shallow diffusions (~ 1 µm) help reduce the effective size of sources and drains. Coevaporation of Al and Si may be needed to avoid short circuits during the alloying phase. Gate oxide must not be too thin (70... 100 nm) in order to limit gate capacitance.

It can be shown that the smallest possible supply voltage V_B for digital CMOS circuits is about 200 mV [5]. Meanwhile, if the threshold voltage V_T of p and n channel transistors is too low, the residual channel current at zero gate voltage becomes a dominant part of leakage current I_0, and static power consumption is increased. Optimum values of V_T are in the range 0.3...0.5 V. An accuracy of $\pm$ 0.1 V can be obtained by ion implantation of both substrate and wells and by carefully optimized annealing.

Strict control of the whole process is needed to minimize junction reverse currents. They can be kept below 10 nA/mm^2 at 1.5 V and ambient temperature.

Metal gate CMOS was the first MOS technology applied to micropower circuits [6]. It is still used as a standard technology for large scale and low-cost production.

Si-gate is preferred [7] in critical micropower applications mainly because of its self-alignment properties. In addition, chip area may be reduced by extensive use of the polysilicon interconnecting layer whose sheet resistance is usually negligible.

Si-gate technology may be further improved by using polysilicon contacts [8], as illustrated in figure 1. This technique requires one additional mask but allows a substantial reduction of the size and depth of source and drain diffused areas. This may result in a 40-percent reduction of dynamic power consumption. Furthermore, the possibility of linking gates and drains directly with strips of polysilicon helps reduce the chip area.

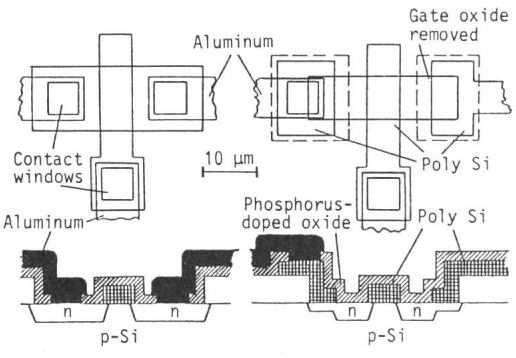

Fig. 1 Standard and polysilicon contact n-channel MOST

Capacitance C can be further reduced by applying local oxidation [9] or silicon-on-sapphire [10...12] technologies. However, these technologies tend to have higher leakage currents, and can thus only be considered for high frequency applications.

Combinations of CMOS and bipolar transistors have been proposed for micro-power applications [13; 14]. Their advantage relies in a higher current handling capability which may be required in the output circuitry.

3. Devices

3.1 Transistors

When the drain current of a MOS transistor is decreased by reducing the gate voltage, the device eventually enters the weak inversion region of operation where the usual parabolic transfer characteristics are no more valid. For long channel transistors with a negligible density of fast surface states and negligible leakage current to substrate, the drain current I_D in weak inversion may be expressed as [15]

$$I_D = S\,I_{D0}\,e^{V_G/nU_T}\,(e^{-V_S/U_T} - e^{-V_D/U_T}) \tag{2}$$

where S is the effective channel width to channel length ratio; V_G, V_S and V_D are the gate, source, and drain potentials with respect to the substrate, and $U_T = kT/q$. The slope factor n ($n > 1$) is fairly controllable, whereas the characteristic current I_{D0} is very sensitive to process parameters and temperature. Both n and I_{D0} may be considered constant for all transistors of a chip biased by values of V_S that do not differ too much from each other.

This model expresses the fact that a MOS transistor in weak inversion is a barrier-controlled device very similar to a bipolar transistor. Drain current I_D becomes saturated as soon as $V_D - V_S$ exceeds a few U_T. By using this behaviour, one obtains an excellent current source. The saturation value of I_D increases exponentially with $-V_S/U_T$ and V_G/nU_T.

The maximum saturation current in weak inversion is roughly given by [15]

$$I_D = \beta\,U_T^2 \tag{3}$$

where $\beta = \mu\,C_{ox}\,S$ is the usual transfer parameter in strong inversion. The maximum value of β achievable with a transistor of reasonable size (0.02 mm^2) is about 10 mA/V^2 which corresponds to a maximum possible operating current in weak inversion of a few µA. For a typical, minimum-sized transistor, this limit is between 10 and 100 nA.

The minimum operating current is limited by carrier generation in the drain and channel depletion layers. It is therefore roughly proportional to the overall area of the transistor. Minimum-sized transistors may be used with a drain current as low as 100 pA at 50 °C.

Small-signal gate to drain transconductance is easily derived from the model as

$$g_m = \partial\,I_D/\partial\,V_G = I_D/n\,U_T \tag{4}$$

Transconductance is proportional to drain current I_D in weak inversion, whereas it is proportional to $I_D^{1/2}$ in strong inversion.

For $V_D - V_S \gg U_T$, a source to drain transconductance may be defined as

$$g_{ms} = -\,\partial\,I_D/\partial\,V_S = I_D/U_T \tag{5}$$

This transconductance is n times larger than that of the gate and is equal to that of a bipolar transistor operated at the same current.

The maximum small-signal amplification achievable with a transistor is limited by the non-zero output conductance g_0 of the device, which is due to channel shortening. As shown in figure 2, this conductance is approximately proportionnal to drain current and characterized by an extrapolated voltage V_E:

$$g_0 \approx I_D / V_E \tag{6}$$

As shown in figure 3, the amplification factor $A_0 = g_m/g_0$ is constant and maximum in weak inversion [16] but decreases like $I_D^{-1/2}$ in strong inversion. This maximum possible gain in weak inversion is a consequence of a maximum value of the transconductance-to-current ratio. It may be further increased by increasing the channel length of the transistor.

Since in weak inversion there is no inverted channel, the major part of the gate capacitance appears between the gate and the substrate and has a value equal to the minimum of the $C_G - V_G$ curve [17]. This value is fairly constant over many orders of magnitude of drain current, and may be 2 to 3 times smaller than the oxide capacitance.

Noise is a limiting factor for transistors used in analog circuits. It may be conveniently characterized by a frequency dependent noise resistance R_n which is a measure of the input noise voltage spectrum. Figure 4 shows typical noise resistances of large transistors integrated in micropower Si-gate technology [17; 18]. At high frequency, shot noise dominates; the noise resistance is independent of frequency and approximately equal to the inverse of transconductance. It increases if drain current is decreased, but it is minimum at a given current if the transistor is in weak inversion.

At low frequencies, flicker noise dominates. The noise resistance is inversely proportional to frequency and to gate area WL. It also depends on the technology through the parameter ϱ.

It may be pointed out that, in the audio frequency range, the noise of the n-channel transistor is independent of drain current down to about 0.2 μA. If gate area is reduced, flicker noise increases and noise stays independent of current up to higher frequencies or down to lower currents. Equivalent input noise voltage of this large-size n-channel transistor integrated over the range 100 Hz to 3 kHz is about 8 μV.

The flicker noise resistance of the p-channel transistor of the same size is about 40 smaller.

3.2 Passive devices

Capacitors are very important in the design of modern analog circuits such as switched capacitor (SC) filters.

In metal gate technology, the best capacitor is the aluminium-gate oxide-diffusion structure which yields a specific value of 300...500 pF/mm². This structure is not available in standard Si-gate technologies due to the self-alignment of gate and diffusions. Nevertheless, a very good capacitor is obtained between the polysilicon and aluminium layers. The vapor-deposited oxide used as the dielectric is thicker than the gate oxide, which reduces the capacitance per unit area to about 100 pF/mm². Matching to $1^0/_{00}$ may be obtained with capacitors of a few picofarads [19].

There is no high resistivity layer available to realize high value resistances. The best layer is the p-well diffusion which reaches 5 to 10 kΩ/□ and allows the realization of a few 100 kΩ on the chip with an accuracy of ± 20%. This value is much too low for most micropower applications. Higher values may be obtained by lightly doped poly Si-layers, but tolerances become very large for sheet resistivities above 1 MΩ/□.

An interesting feature of most Si-gate processes is the availability of both p and n type polysilicon layers [7]. It allows the realization of the lateral polysilicon diode shown in figure 5 [20; 21]. This diode is perfectly isolated from the substrate by the field oxide layer.

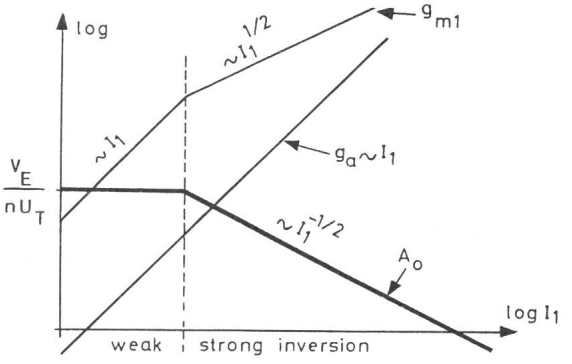

Fig. 3 Amplification factor

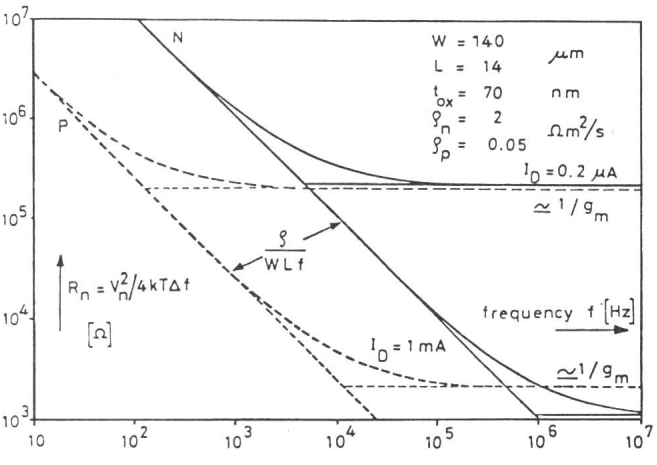

Fig. 4 Noise resistance of MOS transistors

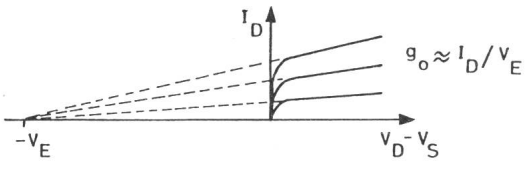

Fig. 2 Output conductance

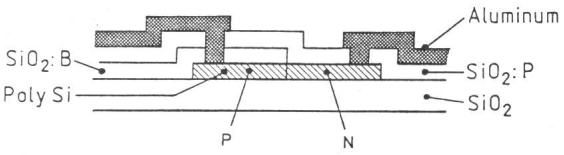

Fig. 5 Lateral polysilicon p–n diode

An important application of this device is the realization of high impedance on-chip voltage multipliers for driving non-volatile memories [22; 23]. It can also be used near the origin of its $I - V$ characteristics as an equivalent resistance of very high value for biasing gates. A 10 µm wide device has an equivalent resistance ranging from 1 to 100 GΩ. It can also be applied to maintain a logic level against leakage currents [20].

4. Digital circuits

As expressed by relation (1), the power consumption of logic CMOS circuits may be divided into static and dynamic components.

In order to limit the dynamic power consumption, the average number of nodes which transit during any period of time must be kept as low as possible. High frequency synchronous circuits must therefore be avoided and replaced by asynchronous cells. Each cell should have a minimum number of nodes changing state to achieve a given function. It should furthermore contain a minimum number of minimum sized transistors in order to obtain a low total parasitic capacitance. Logic structures with critical races must therefore be discarded in favour of race-free circuits which work independently of their delays [24].

As an example, figure 6 shows a race-free divide-by-2 cell [7; 25] made up of 5 gates, and which has a single input I. The behaviour of this structure is described by the set of equations which defines the 5 internal variables A to E (output nodes of the gates). The graph of transitions represented on the same figure shows that no more than one variable tends to transit in any given state, hence there can be no race between variables. Each internal variable transists at half the frequency of the input and may thus be used as output of the divider. Since some transistors can be shared by two gates, the total number of transistors per cell is 19.

Careful analysis of this circuit shows that only some of the transistors are necessary to change the state of the internal variables. The remaining transistors are required to maintain the established states against leakage currents, and may thus be dropped for high frequency circuits. This results in the 9-transistor circuit drawn in solid lines in figure 7 [7]. This dynamic version [26; 27] consumes less than half the dynamic power of the static version. Typical values are 0.4 µA/MHz at 1.4 V.

The same principle has been efficiently applied to all kinds of logic cells. It is not really limited to high frequencies, but can be applied as well to low frequency circuits driven by short logic pulses. For example, by keeping the 4 transistors represented by dashed lines in figure 7, the stable states for I = 0 are maintained and the 13-transistor circuit operates with short 0 input pulses I of arbitrarily low frequency [20]. This semidynamic scheme helps reduce both power consumption and chip area.

Power may be further reduced by feeding the circuit through a voltage reducer at a voltage close to the sum of p and n thresholds [28]. If the voltage of the energy source is sufficient, various parts of the circuit may even be connected in series [11].

Design complexity and chip area of LSI circuits are greatly reduced by replacing random logic by array logic. The latter can be applied in a quite conventional way to low frequency micropower circuits by taking advantage of the two types of

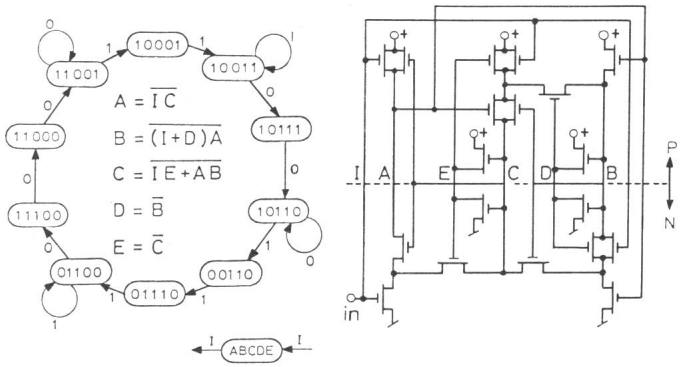

Fig. 6 **Race-free divide-by-2 cell**

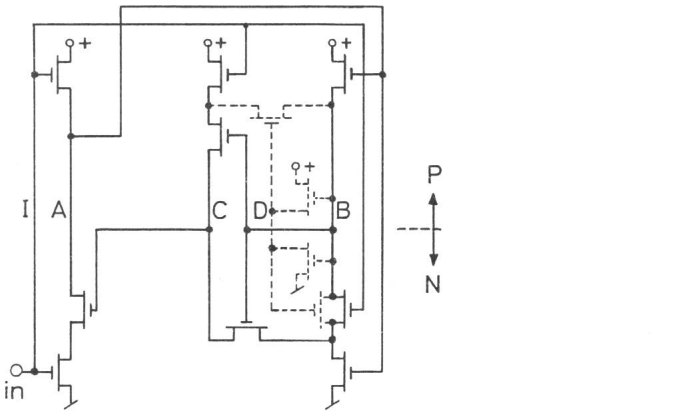

Fig. 7 **Dynamic and semidynamic divide-by-2 cell**

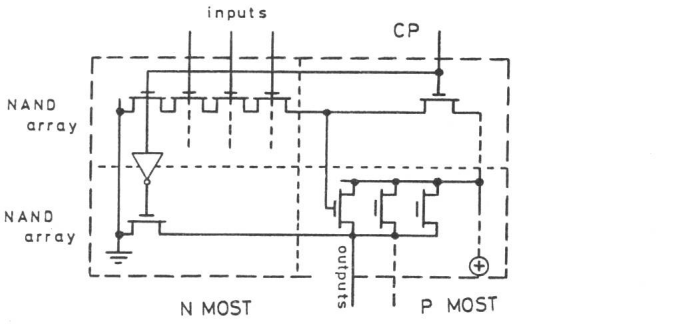

Fig. 8 **CMOS dynamic PLA**

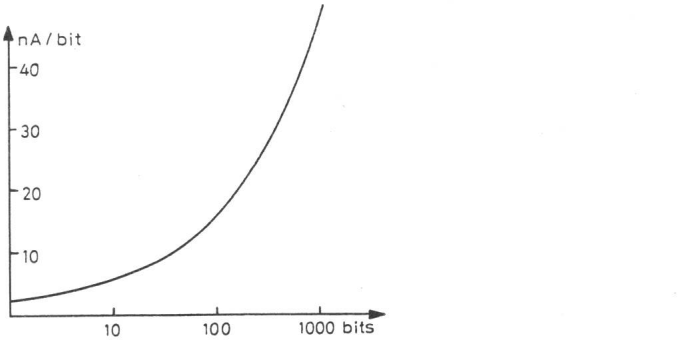

Fig. 9 **Power consumption of a dynamic RAM**

transistors available in CMOS technology [29; 30]. Figure 8 shows the example of a dynamic PLA combining two NAND arrays, that is controlled by a single clock according to the clocked-CMOS principle [31]. Such configurations may be used directly or as a full ROM with the addition of an output multiplexer. A 1-kbit dynamic ROM occupies about 1 mm² in 6 µm technology and consumes approximately 1 nJ at 1.5 V for reading 1 word. This limits the read frequency to 1 kHz for a power consumption of 1 µW. ROMs of this size or more are needed in microprocessor circuits for watches [32; 33].

Micropower static RAMs use standard 6-transistor CMOS cells. Typical power consumption is of the order of 1 µW at 1.5 V for a read/write rate of 5 words/ms. It could be reduced by segmentation of the memory, which reduces the capacitance that must be charged during each read/write cycle. Total area of a 1-kbit static RAM in standard 6 µm technology is about 10 mm².

The standard way of reducing the area of a RAM is to use a dynamic single-transistor cell, which must be periodically refreshed. The calculated current required to charge the capacitance of the selection lines during each refresh cycle is shown in figure 9, assuming a refresh frequency of 5 kHz and a 1.5 V supply voltage [29]. Typically, a 1-kbit dynamic RAM would consume 40 µA, which is inacceptable for most micropower applications. Paradoxically, this dynamic power consumption can be reduced by increasing the storage capacitance. The refresh frequency may then be decreased whereas capacitance of the selection lines stays fairly constant. The price to pay is an increase in size.

5. Analog circuits

Although analog circuits do not usually occupy large areas on micropower LSI chips, they may need a large part of the available power and must therefore be carefully optimized in this respect. This is usually done by using simple configurations to implement the power consuming parts of the circuits [34].

One of the first analog micropower circuits was the quartz oscillator included in every electronic watch. This circuit was consuming most of the power in some early superficial designs [25]. Figure 10 shows the full diagram of a circuit carefully designed for a 32-kHz quartz resonator [35]. The quartz resonator, the transistor T_1 and the two capacitors C_1 and C_2 constitute a simple Pierce oscillator. T_1 operates in weak inversion, where the drain current required to reach the critical transconductance is minimum. Its gate is biased by a single floating polycrystalline diode D_1, which allows DC isolation from the quartz pin Q_1 by a small capacitance C_6. The drain current I_D is supplied by an amplitude regulator [15; 34], which also uses polycrystalline diodes to replace high-value resistors. The resistor of the non-critical low-pass filter D_3 – C_4 is implemented as a symmetrical quad of diodes, to avoid any rectifying effect. This regulator is based on the exponential transfer characteristics of T_3 and T_5 operating in weak inversion. Its output current I_D drops sharply when the amplitude of oscillations coupled through C_7 reaches a critical value. The amplitude of oscillations is thus stabilized at this critical value, which depends solely on $n U_T$ and on the shape factors S of transistors $T_3 ... T_6$. An amplitude of about 150 mV is chosen to limit current drain and distorsions in T_1. Amplification is thus needed to drive logic frequency dividers. It is achieved

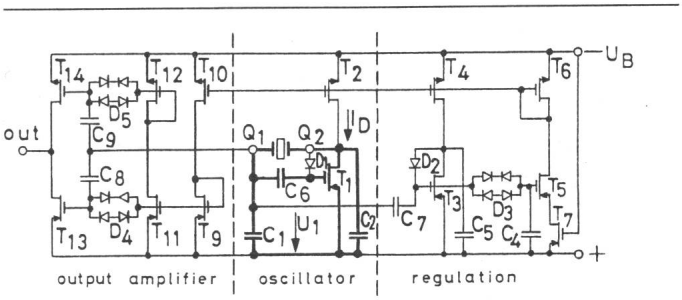

Fig. 10 Quartz oscillator with amplitude regulation

with a minimum amount of power by the complementary transistors T_{13} and T_{14}, which are separately biased close to their thresholds by means of transistors $T_9 ... T_{12}$. The oscillating signal is capacitively coupled to this amplifier through C_8 and C_9. Equivalent resistances D_4 and D_5 avoid that the oscillator be loaded by T_9 and T_{12}. All coupling capacitors have values below 2 pF.

As shown in figure 11, the total current consumed by this oscillator is fairly independent of supply voltage V_B. It is of the order of 50 nA and increases by one to two orders of magnitude if the quartz resonator is removed. Total currents lower than 20 nA have been measured with lower values of capacitors C_1 and C_2.

Another example of an analog circuit developed for electronic watches is the voltage reference needed to check the state of the battery. The standard bandgap principle can be applied by using the base-emitter junction of the substrate transistor available in CMOS technologies to realize the diode. A compensation voltage proportional to absolute temperature is obtained by means of the bipolar-like transfer characteristics of MOS transistors in weak inversion [36; 37; 38]. Voltage stability better than ± 10 mV is easily achieved in the range −20...+80 °C, but initial adjustment at room temperature is needed to compensate mismatches of transistors.

Another very interesting solution is based on a transistor pair of the same type, except for the opposite doping type of their polysilicon gates [39]. As shown by figure 12, the gate voltage difference ΔV_G of such a pair is nearly independent of current in weak inversion and is close to the bandgap voltage of silicon. The temperature dependence of the bandgap voltage can be easily compensated by choosing different current densi-

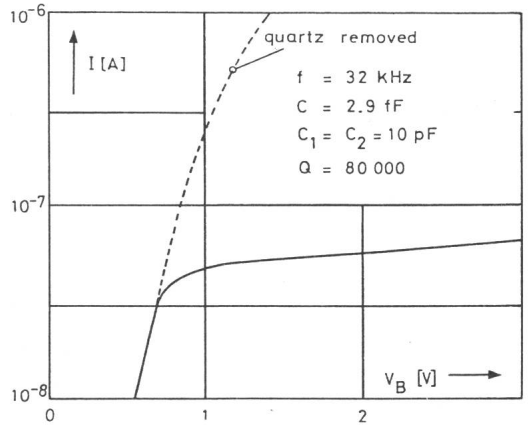

Fig. 11 Current drain of 32-kHz quartz oscillator

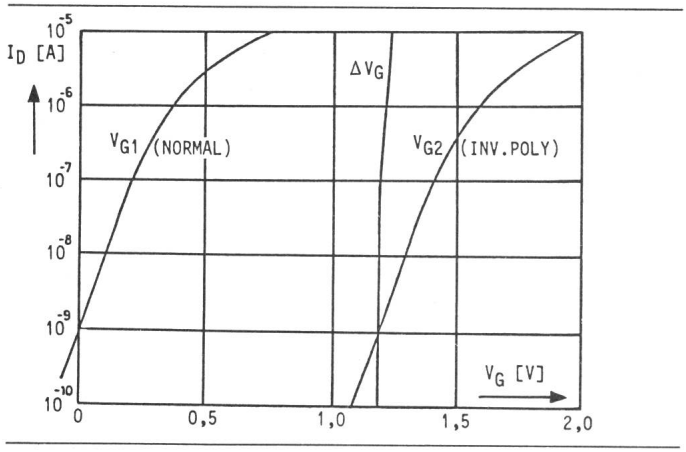

Fig. 12 Gate voltage difference ΔV_G of n-type transistors with n+ (normal) and p+ (inverted) doped gates

ties for the transistors of the pair. Voltage stability of $\pm$ 1 mV has been obtained in the range $-20...+80$ °C, with a total current drain below 100 nA. These excellent characteristics may find applications much beyond that of battery checking.

Switched capacitor filters find applications in micropower circuits for medical electronics, and they will be needed in future portable devices to process analog signals delivered by sensors. Most of the power consumed by SC filters goes into the operational amplifiers. These must therefore be specially designed for very low-power filters [19; 40]. A commonly used circuit is shown in figure 13 [16]. It combines a *n*-channel differential pair $T_1 - T_3$ and a *p*-channel current mirror $T_2 - T_4$ to achieve voltage amplification at high impedance node (a). A *n*-channel source follower T_5 is provided to insure low output resistance. Figure 14 shows the measured frequency dependence of the gain A of such an amplifier driven at the negative input, with $2\,I_1 = 0.1$ µA, $I_2 = 1$ µA and a total capacitive load $C_c = 5$ pF at the output node (c). This circuit behaves essentially as an integrator with a time constant

$$\tau_1 = C_a/g_{m1} \tag{7}$$

where C_a is the capacitance loading node (a) and g_{m1} the transconductance of transistors T_1 and T_3. It has a significant pole due to the time constant

$$\tau_2 = C_c/g_{m5} \tag{8}$$

at output node (c).

Since the amplifier operates in weak inversion, a fairly high voltage gain A_0, close to 60 dB, is obtained with a single stage, and therefore no compensation is needed for any amount of voltage feedback smaller than 1. This amount of feedback is always close to 1 in most SC filters. The settling time T_s necessary to reach equilibrium with a residual error ε may then be approximated by [19]:

$$T_s \cong (\tau_1 + 2\,\tau_2)\,\ln \varepsilon^{-1} \tag{9}$$

In a SC filter, all the high frequency noise is transposed to low frequencies by undersampling. For this reason, white shot noise predominates at low currents, even though $1/f$ flicker noise is dominant in the audio part of the spectrum in the absence of sampling. The noise bandwidth of the amplifier can be shown to be independent of τ_2 and equal to

$$\Delta f = {}^1/_4\,\tau_1 \tag{10}$$

The equivalent shot noise resistance R_n may be expressed as

$$R_n = \frac{V_n^2}{4\,kT\Delta f} = \gamma/g_{m1} \tag{11}$$

where $1 < \gamma < 4$ depends on the relative contribution to the noise of transistors T_1 to T_4. Combination of (7), (10) and (11) yields

$$V_n^2 = \gamma\,kT/C_a \tag{12}$$

Equivalent noise voltage at the input of the amplifier depends thus almost solely on the value of capacitance C_a at amplifying node (a). The maximum possible value of C_a is limited by the settling time T_s given by (9), which must be shorter than the half sampling period ${}^1/_2$ fc. Application of this condition yields

$$V_n^2 > 2\,kT\frac{f_c}{g_{m1}}\gamma\,\ln \varepsilon^{-1} \tag{13}$$

Due to the requirement on settling time, the minimum possible shot noise component is thus inversely proportional to transconductance g_{m1}; it is therefore increased at low current.

Figure 15 shows as an example the circuit diagram of a second order, stray-insensitive filter which has been realized for micropower applications [19]. This filter consumes less than 10 µW at 3 V with a resonant frequency at 1.4 kHz. Measured dynamic range is 51 dB, but calculations show that

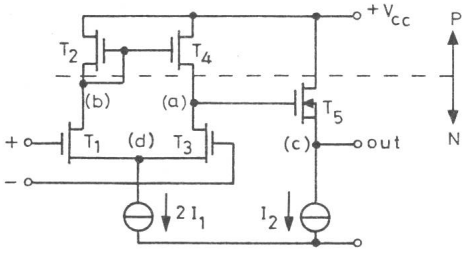

Fig. 13 Simple operational amplifier

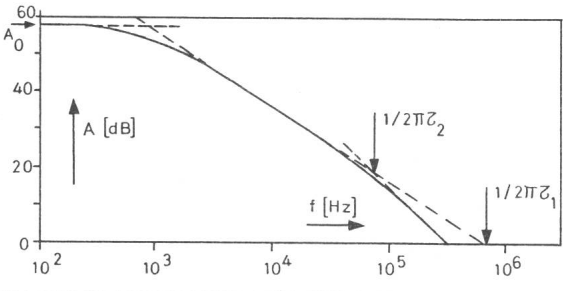

Fig. 14 Gain of operational amplifier

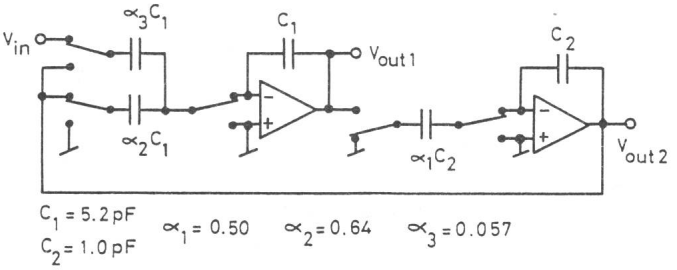

Fig. 15 Second order stray-insensitive filter

it can be extended to above 60 dB by slightly modifying the amplifiers. Power could be further reduced by using dynamic amplifiers [41; 42; 43].

6. Systems

Constraints in the realization of complete LSI micropower systems result from the limitations of the subcircuits.

Minimum dynamic power consumption is always achieved by asynchronous circuits, which must therefore be used for high frequency logic functions. The average clock frequency of synchronous processing circuits must be as low as possible. This requires special architectures that allow, for example, to suppress the clock after completion of each operation [32; 33; 44; 45]. Maximum clock frequency is limited by low supply voltage. Fast functions must thus be committed to special peripheral circuits.

Integration of most of the parts of a system on a single chip is desirable, in order to reduce the number of power consuming interfaces, and to save space which is often limited in battery operated instruments.

Fast signal processing must be achieved by analog circuits which have to be carefully designed with respect to power consumption.

Latch-up effects which plague many CMOS circuits may be easily avoided by the addition of a single integrated series resistance which limits the current below the holding value (of the order of 1 mA), but which has a negligible effect at nominal current. Battery operation isolates the chip from various noise and impulse signals usually delivered by power networks.

Good examples of micropower capability are given by watch circuits operating at 1.5 V with a standard 32 kHz quartz resonator. Microprogrammed circuits intended for LCD digital watches consume 1...6 µA [32]. The best circuits for analog watches need about 0.1 µA. Total current of 2 µA has been reported for a watch circuit designed for 4.2 MHz [28].

7. Conclusion

A variety of digital and analog functions can be implemented within a single LSI chip that consumes a few µW or less, provided fundamental constraints on speed, bandwidth and dynamic range are accepted. The degradation of performances is less than proportional to the reduction in power consumption. This results from special circuit schemes, some of which take advantage of MOS transistors operating in weak inversion. Future improvements will be made possible by further refinement of circuit and system designs, and by the availability of submicron technologies boosted by worldwide efforts towards VLSI.

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